DDC / DUC
Since 2006

What is OpenHPSDR?

Open
High
Performance
Software
Defined
Radio

- An international group of SDR enthusiasts.
- Developing open-source hardware and software.
- Very "High Performance" designs --- extending the state of the art of SDR in Amateur Radio.
- Having a lot of fun working with each other, challenging each other, and learning as we develop and test new technology.
- Partners (separate entities) include TAPR and Apache Labs.

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OpenHPSDR Topics Pacificon 2014

NEW ITEMS THAT ARE NOW SHIPPING

- WDSP – New DSP library
- PureSignal – Adaptive pre-distortion
- EER / ET firmware & software

ACTIVE DEVELOPMENT

- New Communication Protocol

ACTIVE INVESTIGATION

- Direct Fourier Conversion & New Architectures

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WDSP

- Developed for our current and FUTURE openHPSDR needs
- Readily useable for other SDR projects
- Many enhanced and new functions
- Open-source, GNU GPL version 2
- C Programming Language – Close to the hardware & Efficient
- Shipping NOW! (But, always opportunities to do more! ☺)

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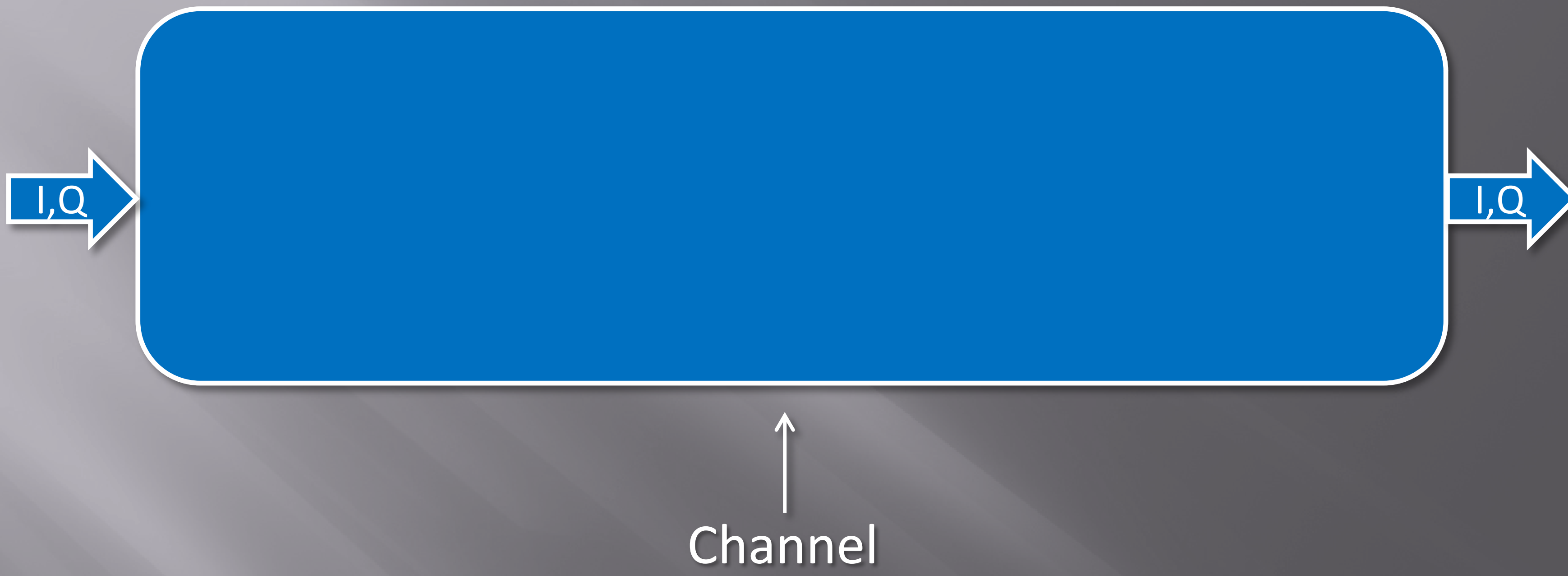
THE CHANNEL CONCEPT



A software entity that accepts buffers of I,Q data and outputs buffers of I,Q data.

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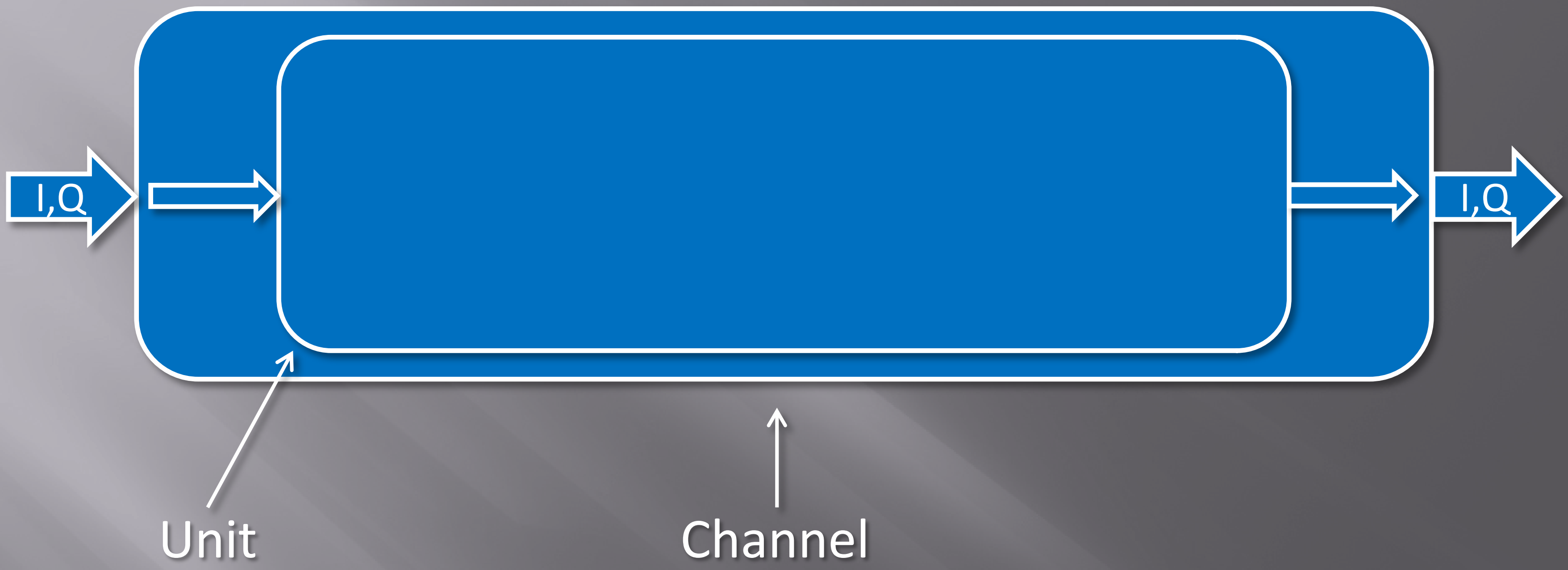
THE CHANNEL CONCEPT



The CHANNEL provides the home for a <u>single</u> UNIT such as a receiver or transmitter.

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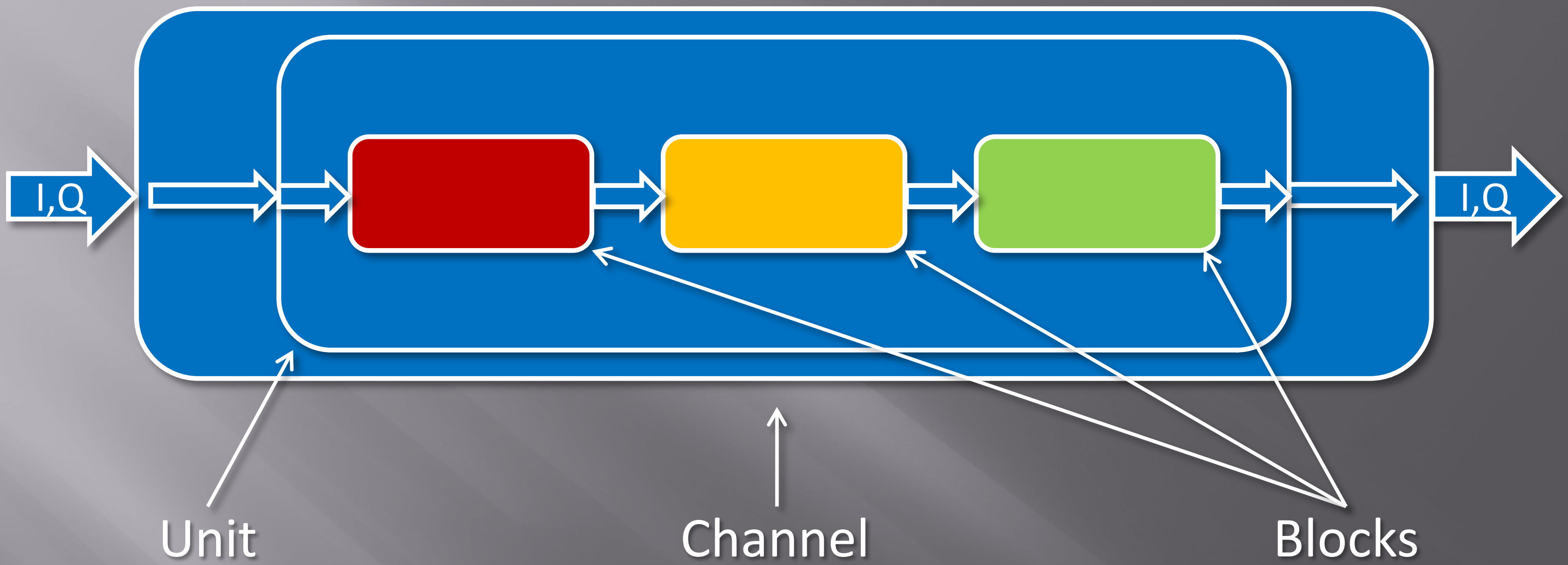
THE CHANNEL CONCEPT



The UNIT comprises BLOCKS, each of which performs a specific function such as Filter, AM Modulator, or ALC.

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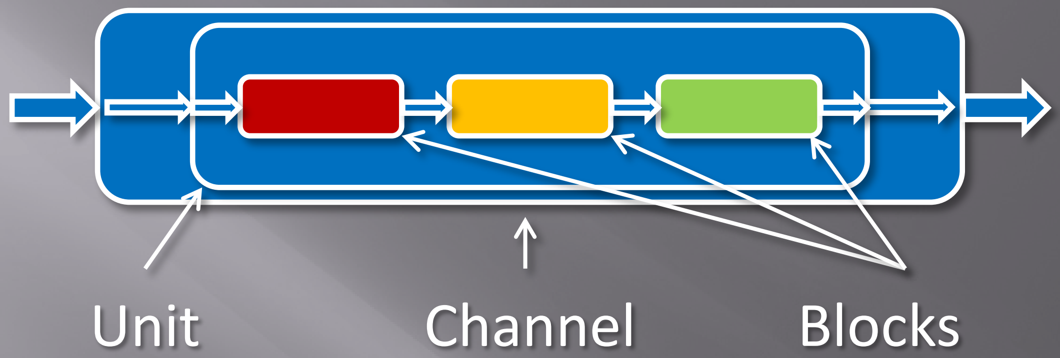
THE CHANNEL CONCEPT



- Each CHANNEL is completely independent of all others – Channels share nothing – No shared data or settings.

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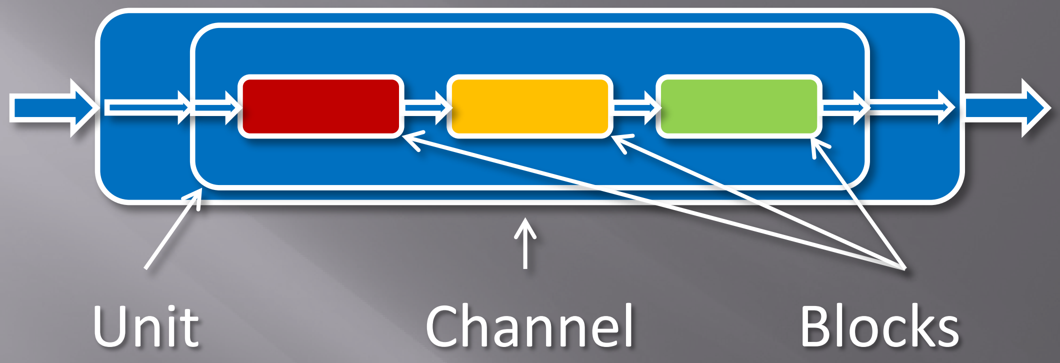
THE CHANNEL CONCEPT



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- You can have as many channels as you want.

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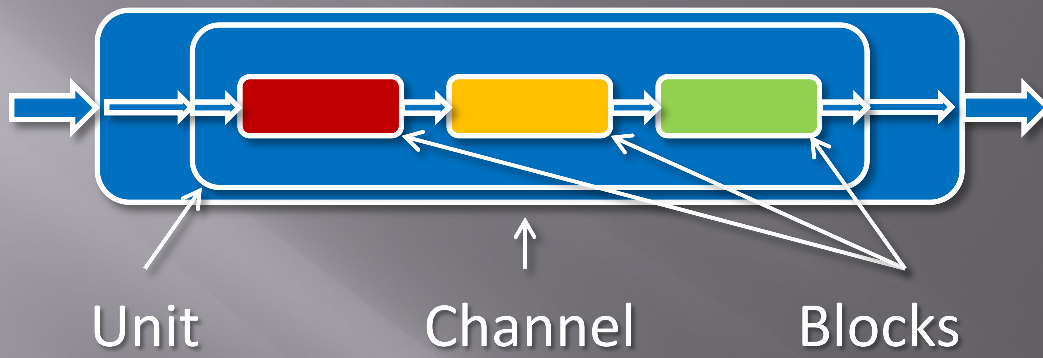
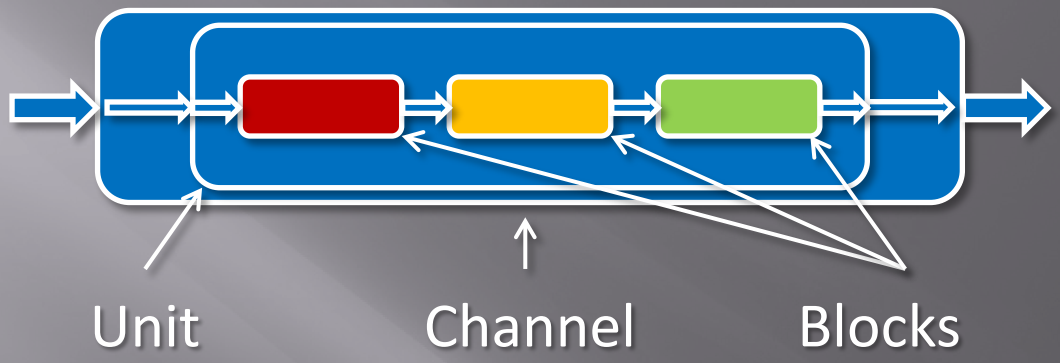
THE CHANNEL CONCEPT



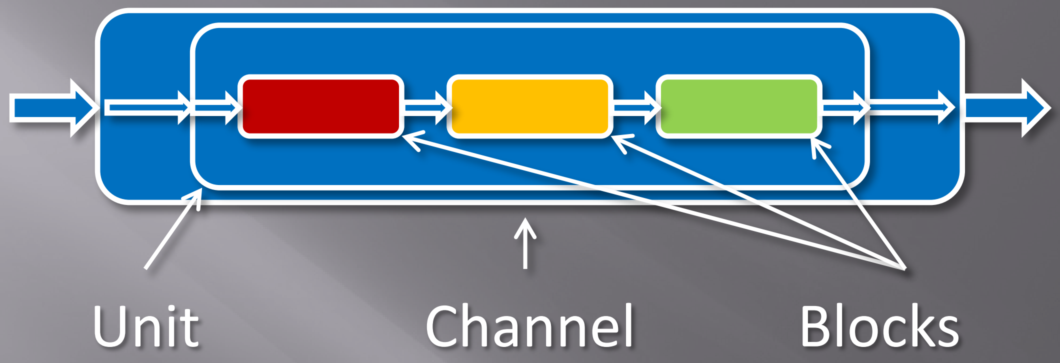
- Each CHANNEL is completely independent of all others – Channels share NOTHING – No shared data or settings.
- You can have as many channels as you want.
- The CHANNEL structure is <u>always exactly the same</u>, no matter what type of unit is housed within it.

THE CHANNEL CONCEPT



- After defining a UNIT, you can use that definition within as many channels as you want.
- Pre-defined units include a Receiver & a Transmitter.
- It is simple to add new types of units – very uniform structure to “splice” them into channels.

THE CHANNEL CONCEPT



- After defining a BLOCK, you can use that definition as many times as you want within a single unit and you can use that definition in other units.
- BLOCKS also have a very uniform structure.

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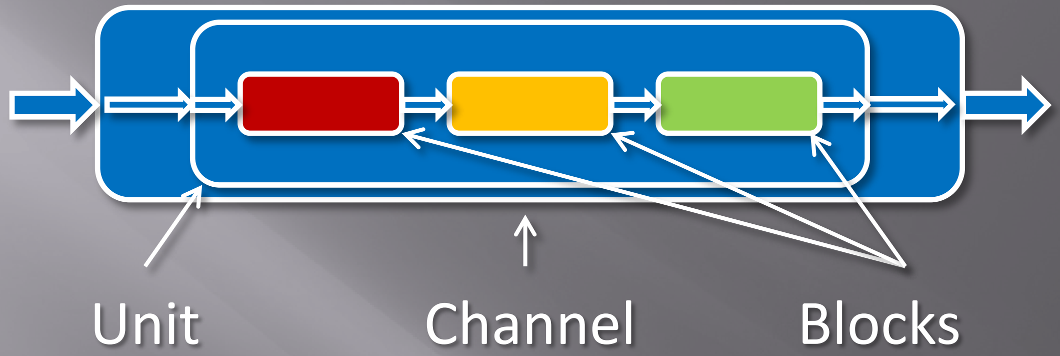
THE CHANNEL CONCEPT



Single CHANNEL structure, uniform UNIT structure, and uniform BLOCK structure support easy re-use of technology and more rapid development.

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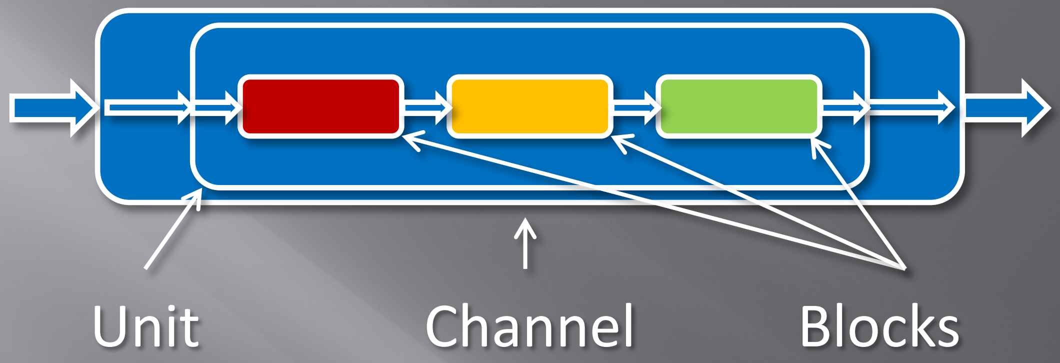
THE CHANNEL CONCEPT



A rich assortment of BLOCKs has been included!

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WDSP
AVAILABLE BLOCKS

- Frequency-shifter (complex oscillator + mixer)
- Resampler
- Signal Generators
  - sine, pulse, two-tone, triangle, noise, sawtooth
- Adjustable bandpass filters
- AM squelch & transmit noise-gate
  - raised-cosine transitions
  - continuously variable tail length
- AM Demodulation
  - basic & synchronous modes
  - sideband selection (lower, upper, or both) – true phasing separation, not filtering
  - carrier stabilization

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WDSP
AVAILABLE BLOCKS

- FM Demodulation
  - de-emphasis
  - CTCSS block
- FM Squelch
  - raised-cosine transitions
  - continuously variable tail length
- Equalizer
  - continuous-gain (as opposed to gain by band)
  - specify gain at any number of frequencies
- Automatic Notch Filter (LMS algorithm)
  - automatic variable leak
- Automatic Noise Reduction (LMS algorithm)
  - automatic variable leak

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WDSP
AVAILABLE BLOCKS

- Speech processor
  - characteristics of an RF speech processor
- AM modulator
  - zero carrier shift
  - absolute 100% modulation control available
- FM modulator
  - pre-emphasis (either before or after limiting)
  - CTCSS tones
- Preemptive NoiseBlanker
  - slew time, advance time, hang time control
- Diversity mixing
- PureSignal transmit linearity correction
- Audio Peaking Filters for CW & RTTY

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WDSP
AVAILABLE BLOCKS

- AGC / ALC / Audio Leveler
  - ZERO overshoot (total amplitude control)
  - automatic fast decay mode for transients
  - hang functionality
  - slope functionality (strong stations sound louder)
  - get / set functions for controls on panadapter
- Patchpanel
  - select I or Q or I and Q
  - copy I➔Q or Q➔I
  - mutual and separate I, Q gain controls
  - use for input select, audio pan, binaural output selection, etc.

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WDSP
AVAILABLE BLOCKS

- Meters
  - peak, average, and gain modes
- Phase & scope display
- Panadapter / Spectrum display
  - large FFT support for weak signal
  - stitched spectra for wider display
  - adjustable frame rate (independent of sample rate and FFT size)
  - spur elimination for Cyclops spectrum analyzer
  - resamples to chosen pixel width
  - selection of window functions
  - selection of averaging modes
- AND MORE ...

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OpenHPSDR TOPICS
Pacificon 2014

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ACTIVE INVESTIGATION

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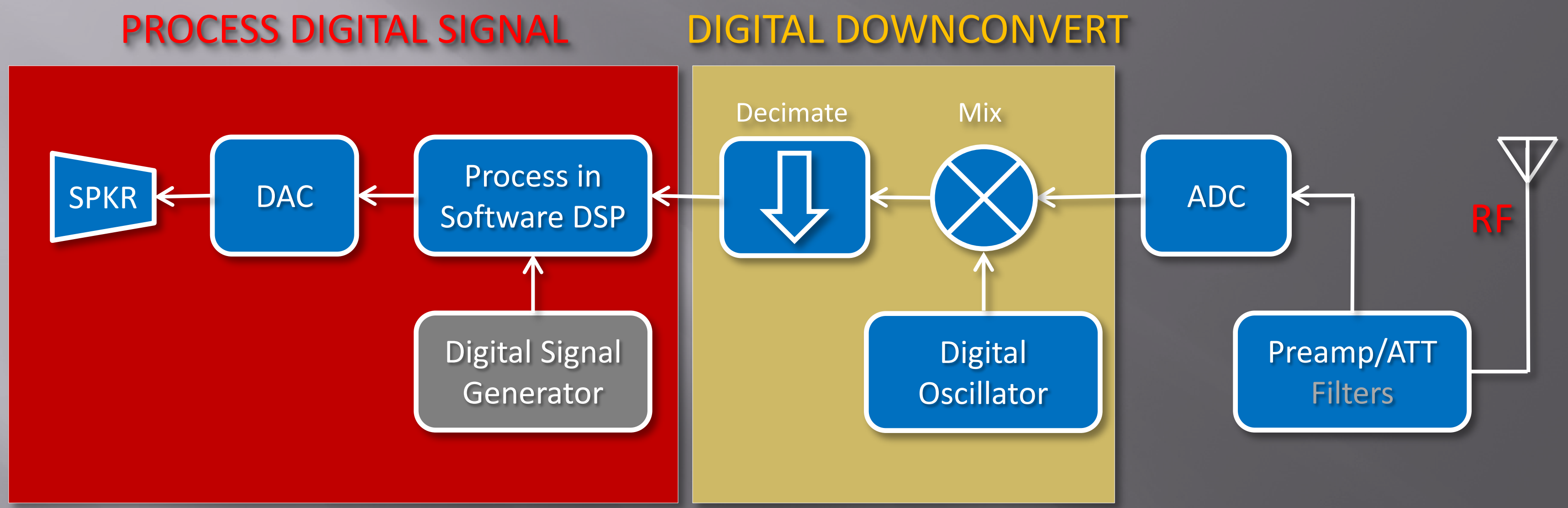
DDC RECEIVER



- Mix With Complex Oscillator To Generate Baseband (0 Hz IF) Signal
- Decimate Down From The Sample Rate Of The Oscillator & ADC (122.88 Mhz)

- Process The Complex Digital Signal (I,Q) To Generate Audio
  - Sample rates are easily processed in software (48K – 384K)

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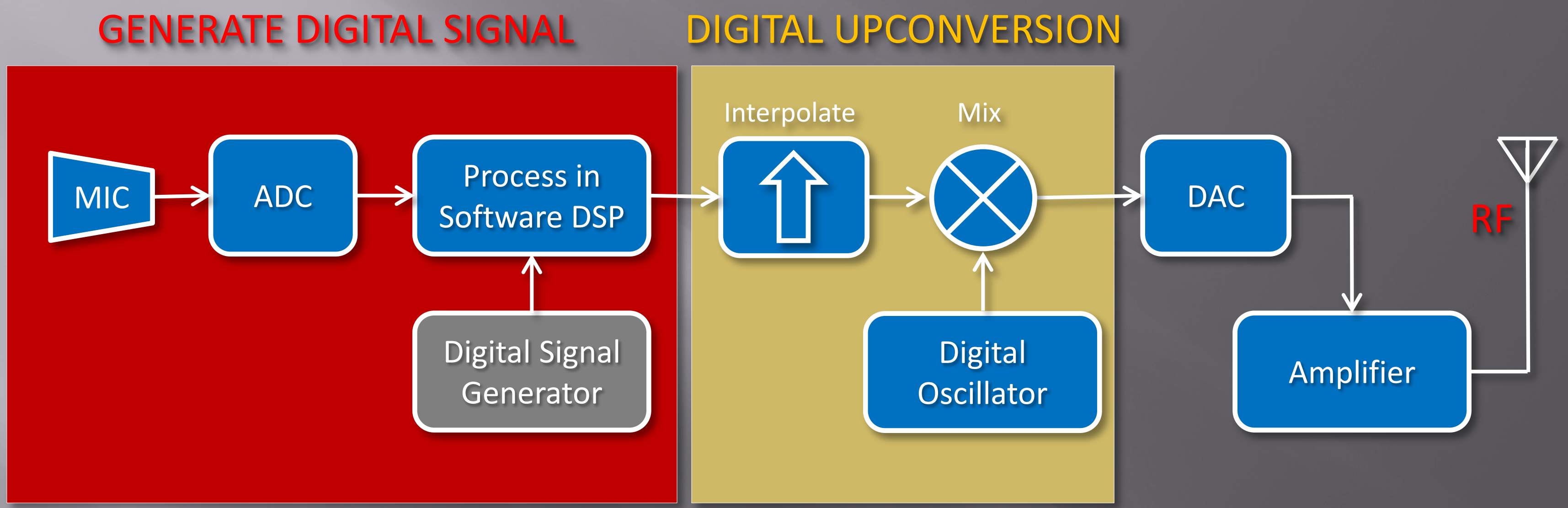
DUC TRANSMITTER



- Complex Digital Signal (I,Q) Generated From Audio Data
  - Sample rates are easily processed in software (48K – 384K)

- Interpolate Up To The Sample Rate Of The DAC & Oscillator (122.88 Mhz)
- Mix With Complex Oscillator To Generate The RF-Frequency Digital Signal

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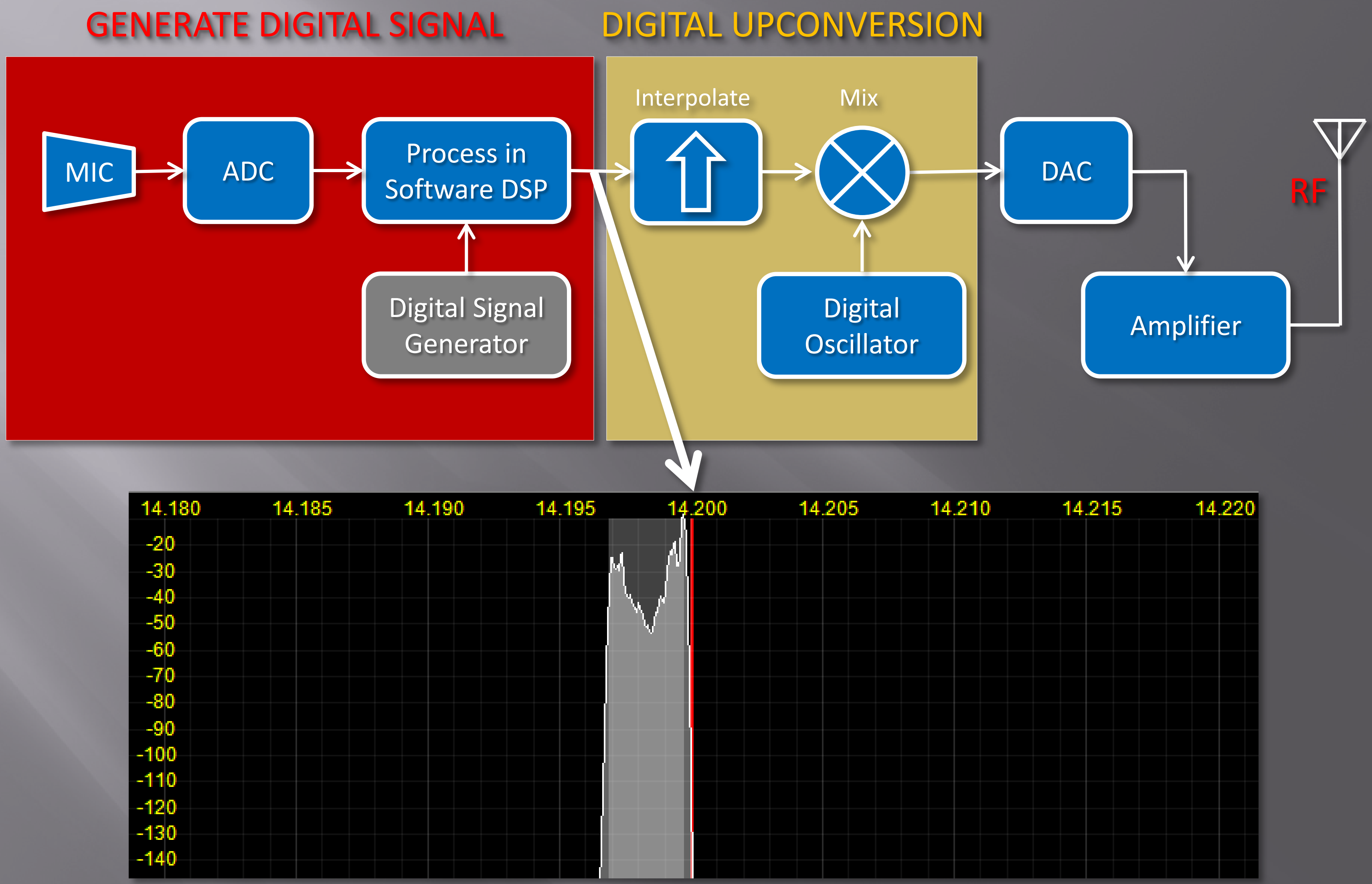
DUC TRANSMITTER



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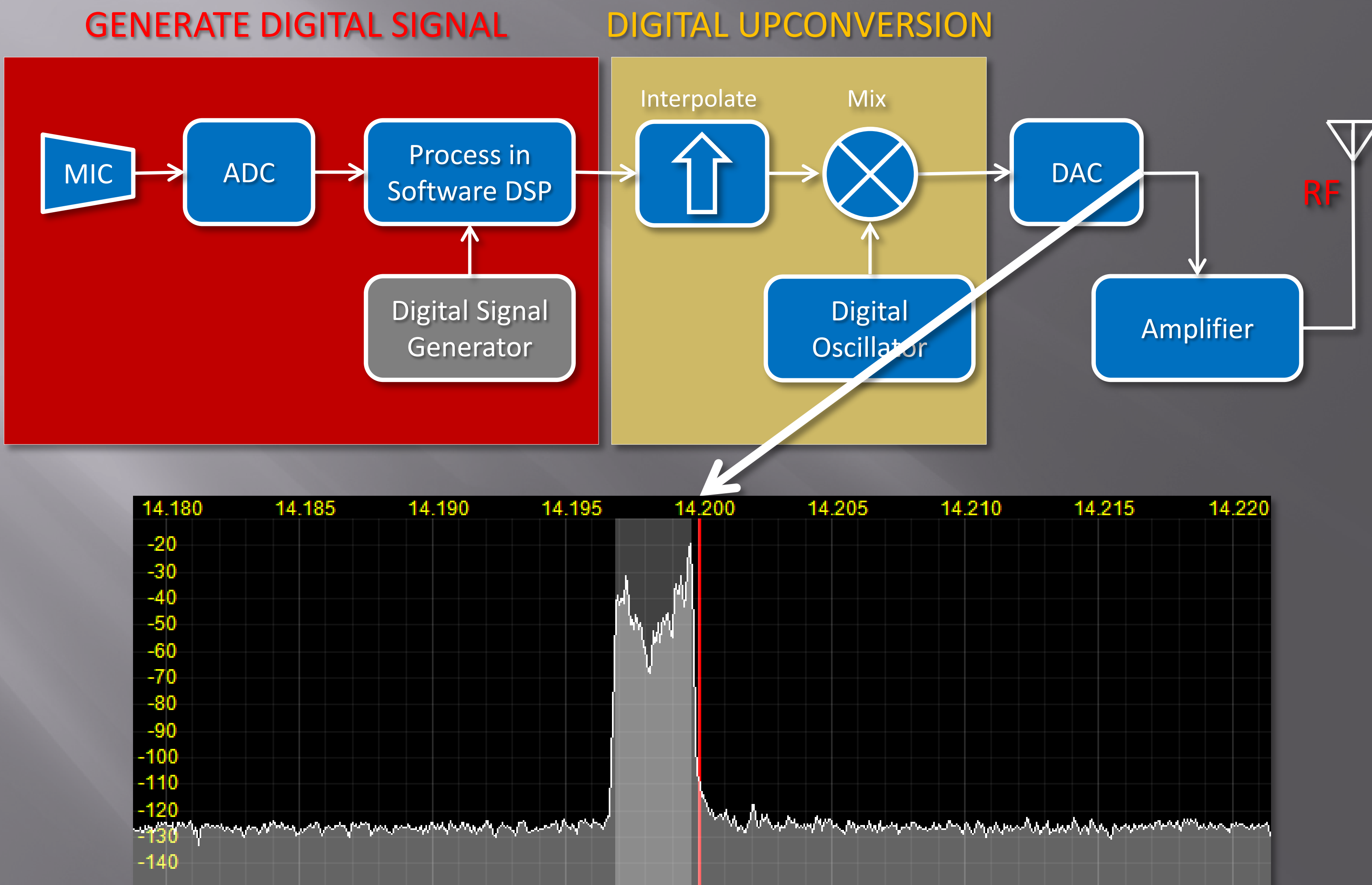
DUC TRANSMITTER



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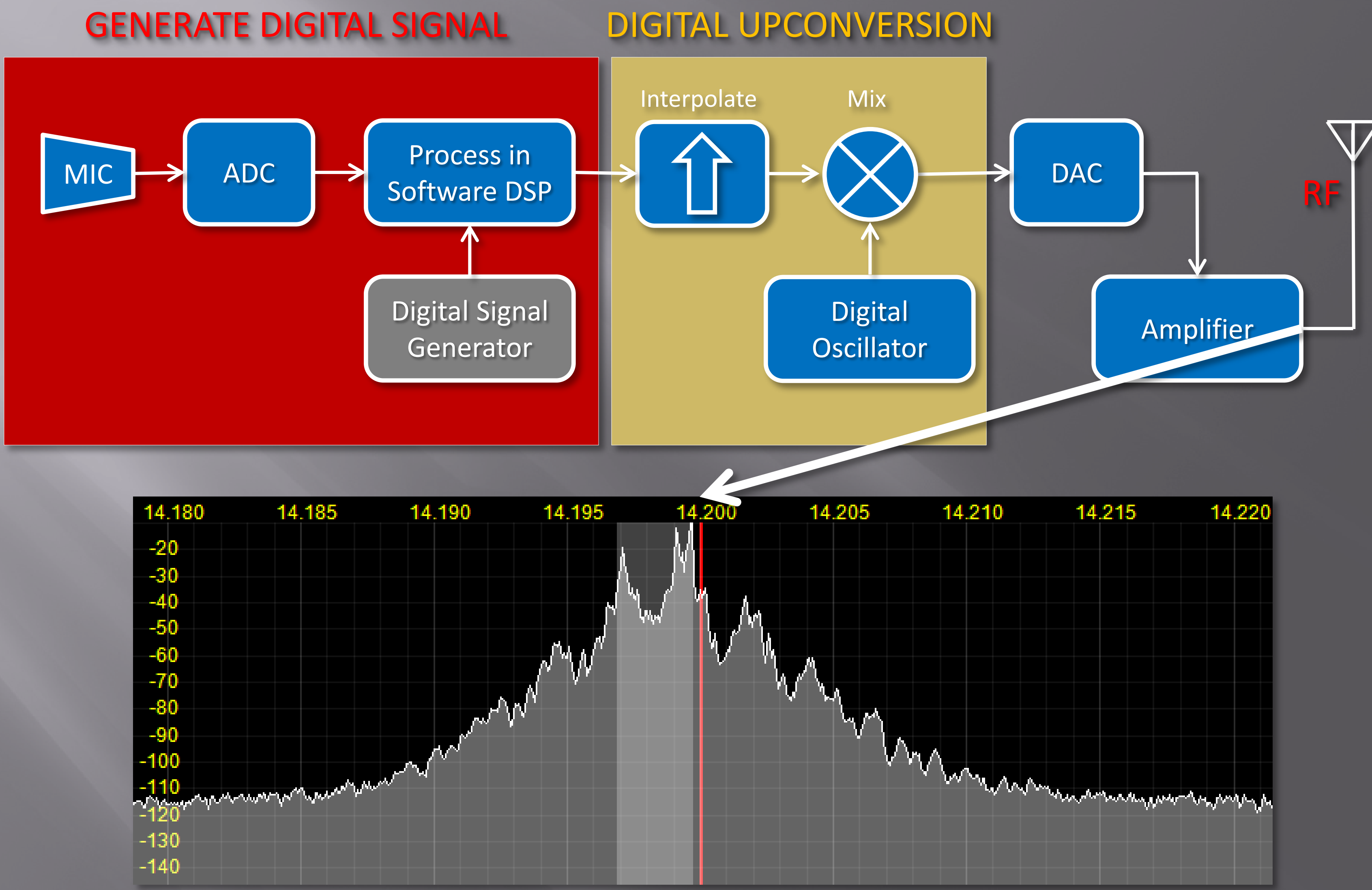
DUC TRANSMITTER



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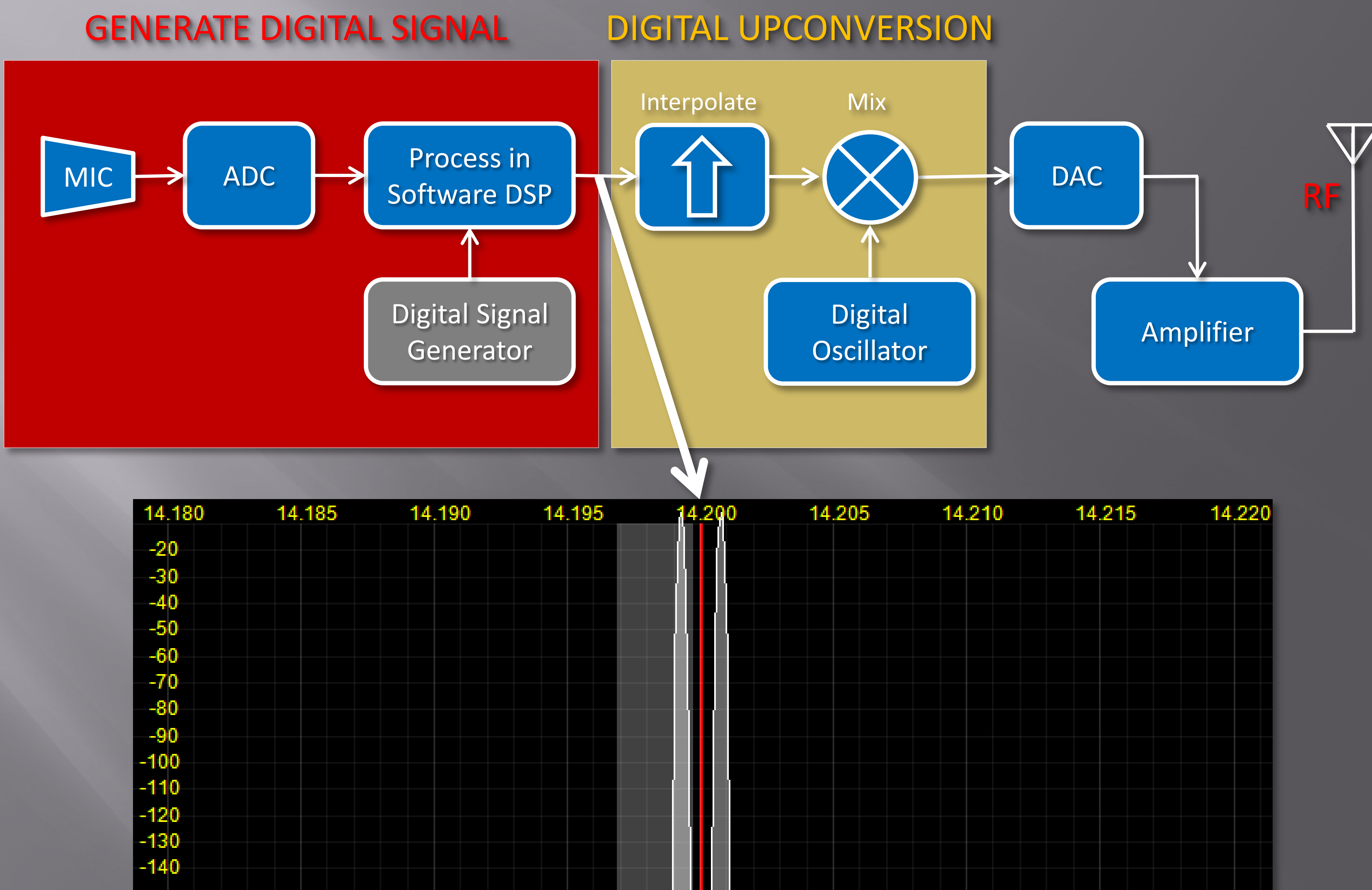
DUC TRANSMITTER



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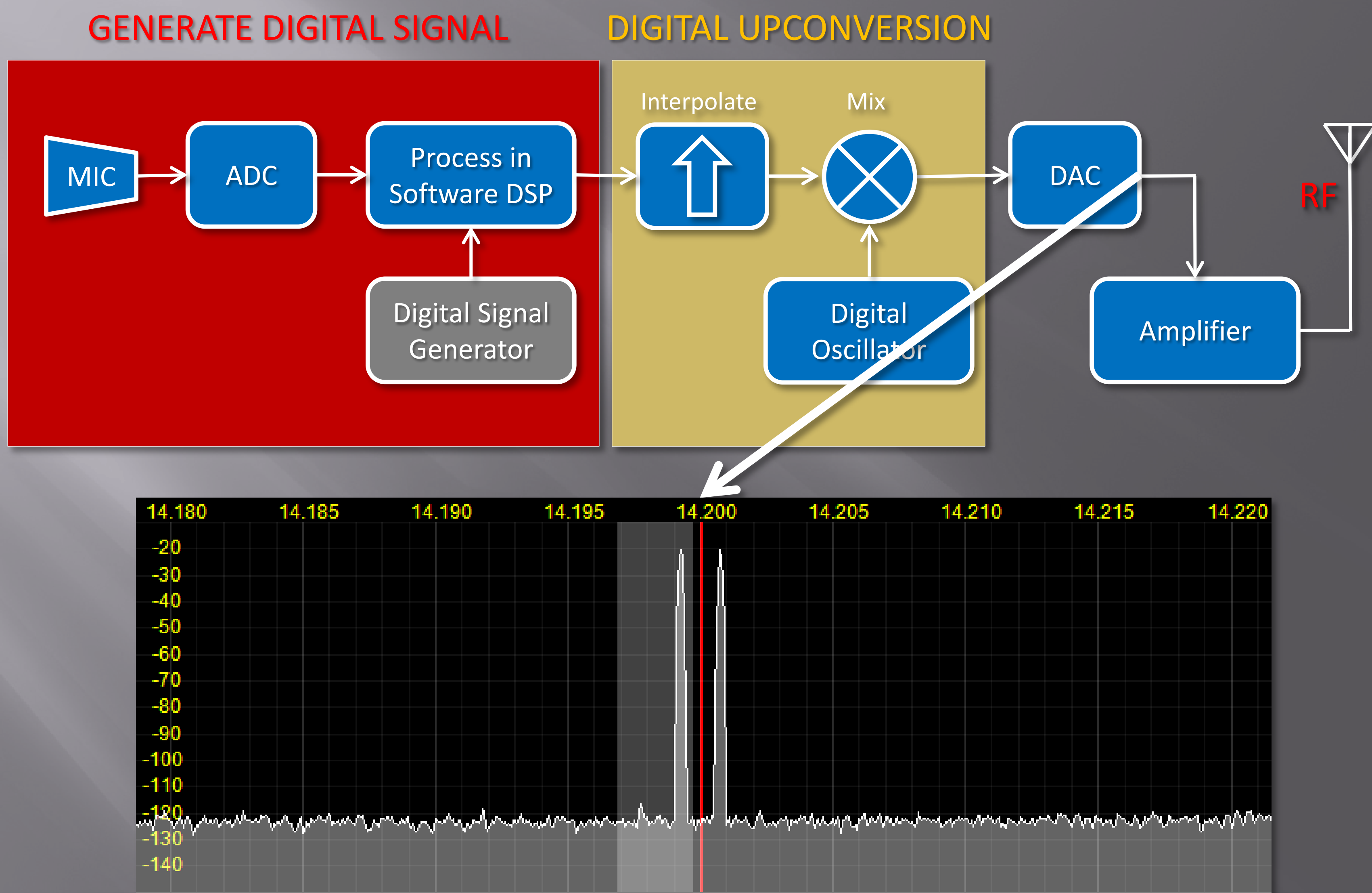
DUC TRANSMITTER



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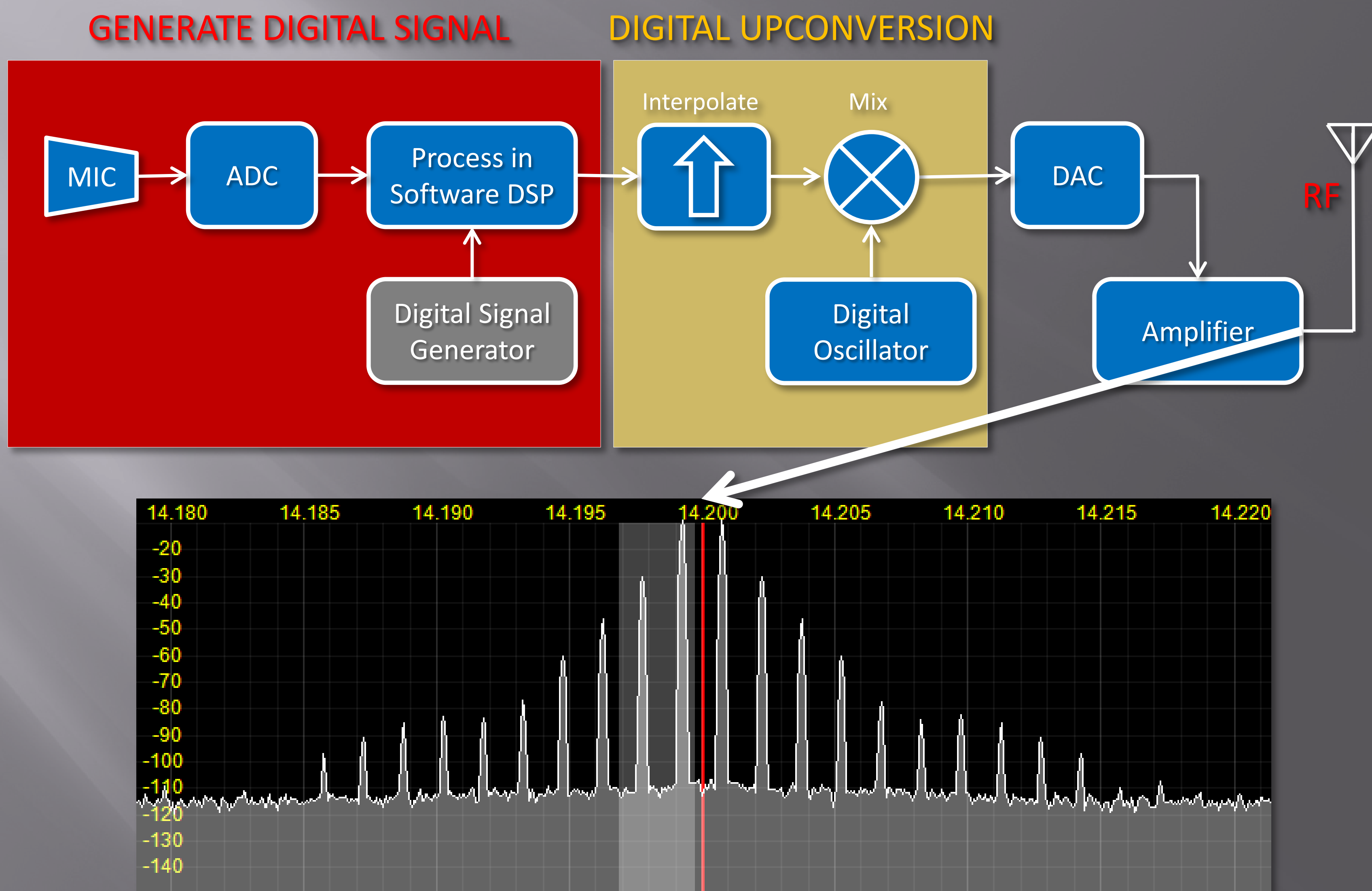
DUC TRANSMITTER



WHY ?

WHY ?

Because the amplifier is NOT perfectly linear!

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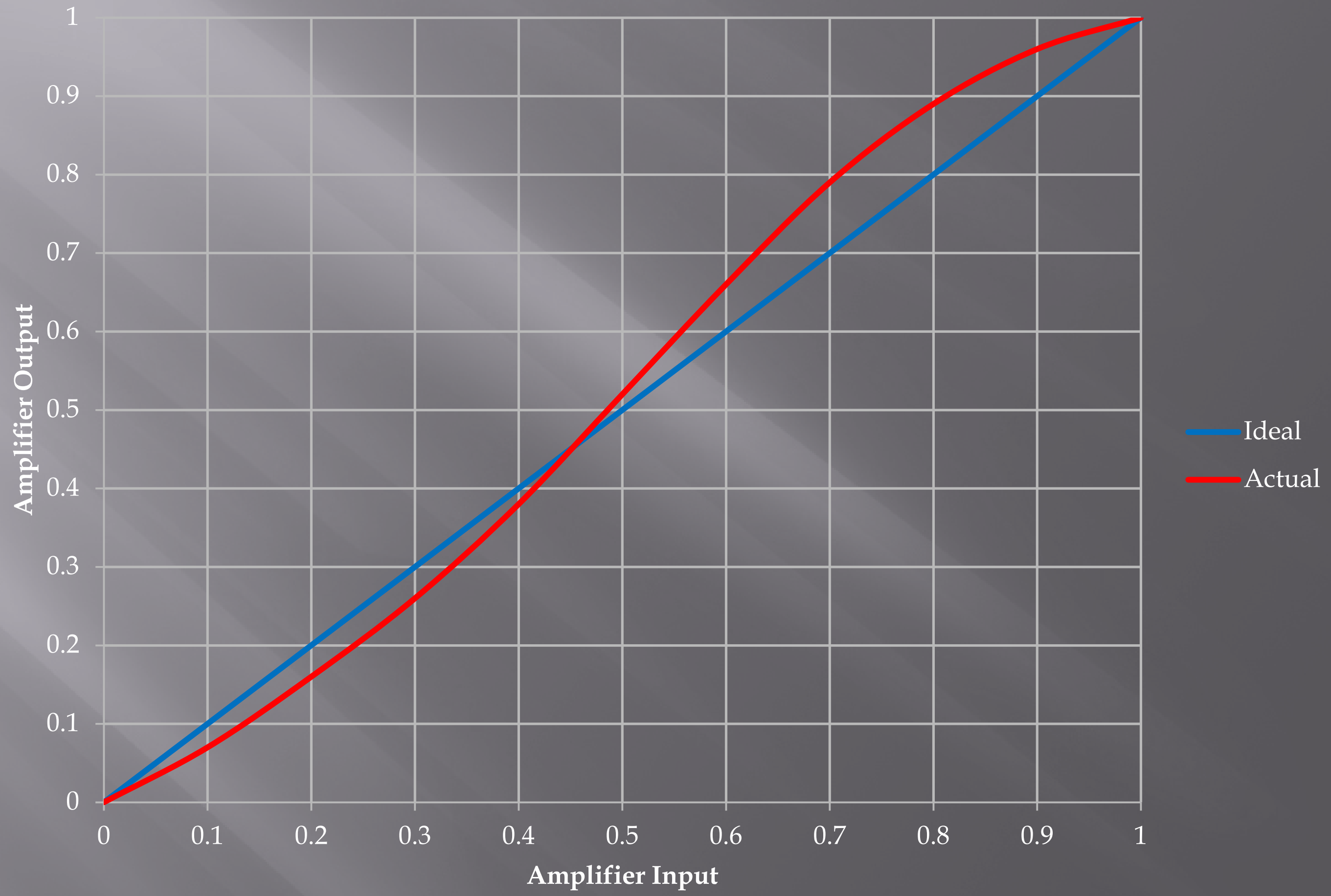
AMPLITUDE NON-LINEARITY



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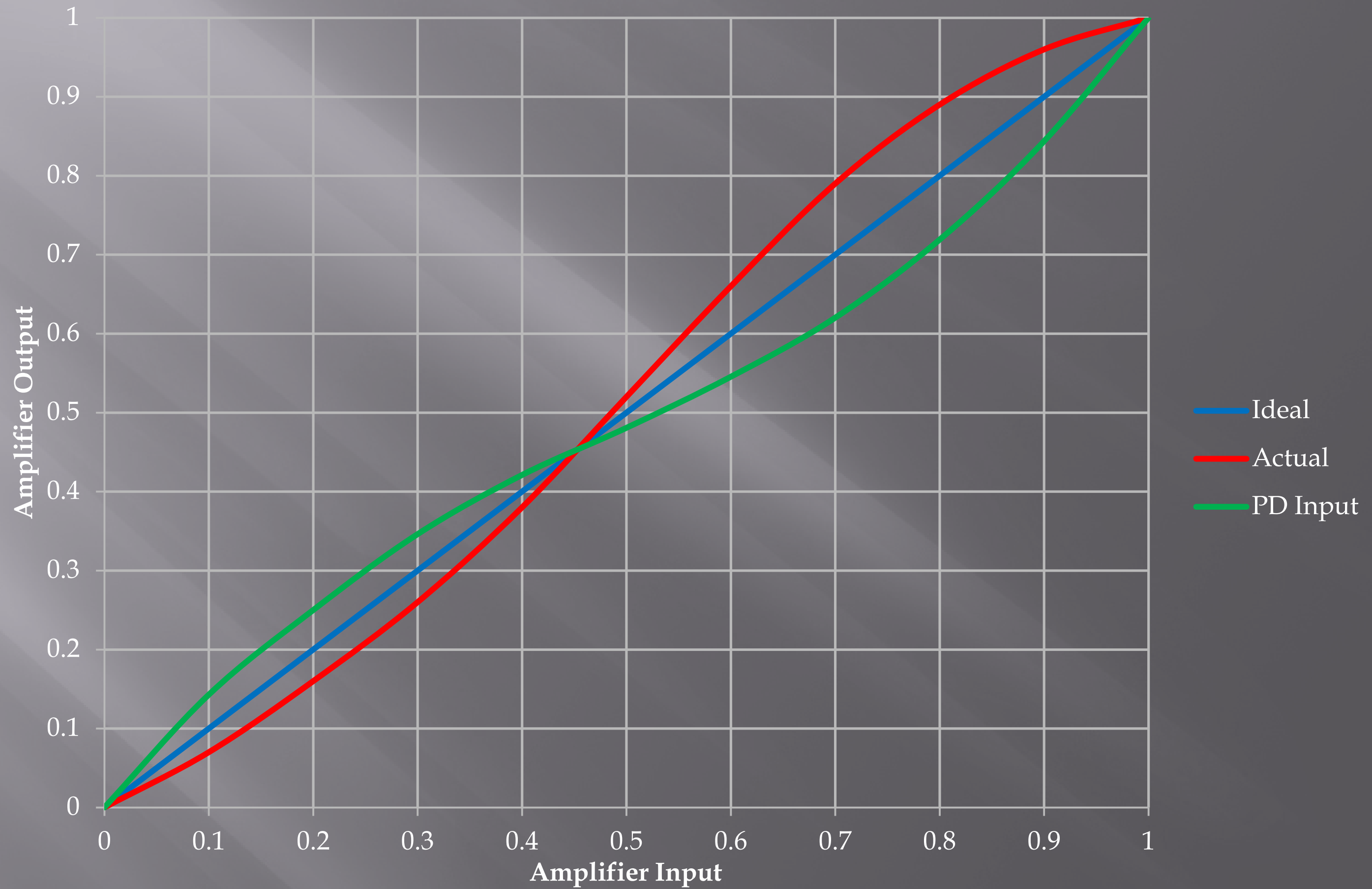
CORRECT BY PREDISTORTION



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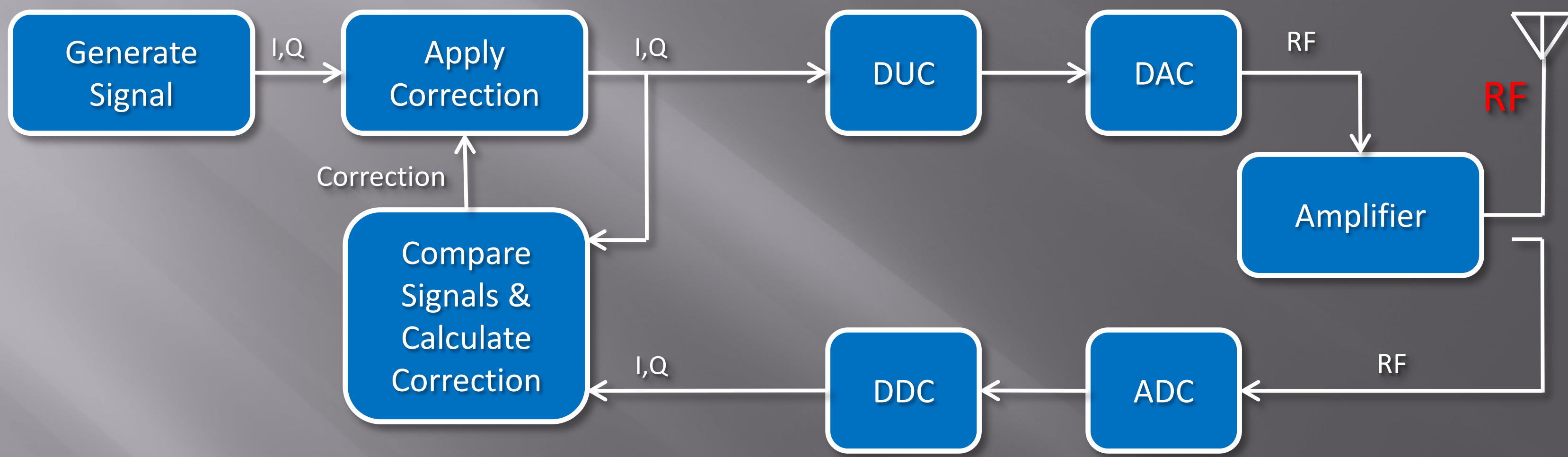
ADAPTIVE BASEBAND PREDISTORTION

Basic Concept



- Apply Correction to the out-bound signal
- Calculate Correction by Comparing the Input & Output of the Amplifier
    - BASEBAND – I,Q Before Up-Conversion / I,Q After Down-Conversion
    - ADAPTIVE – Repeat the process to Adapt to Changing Conditions

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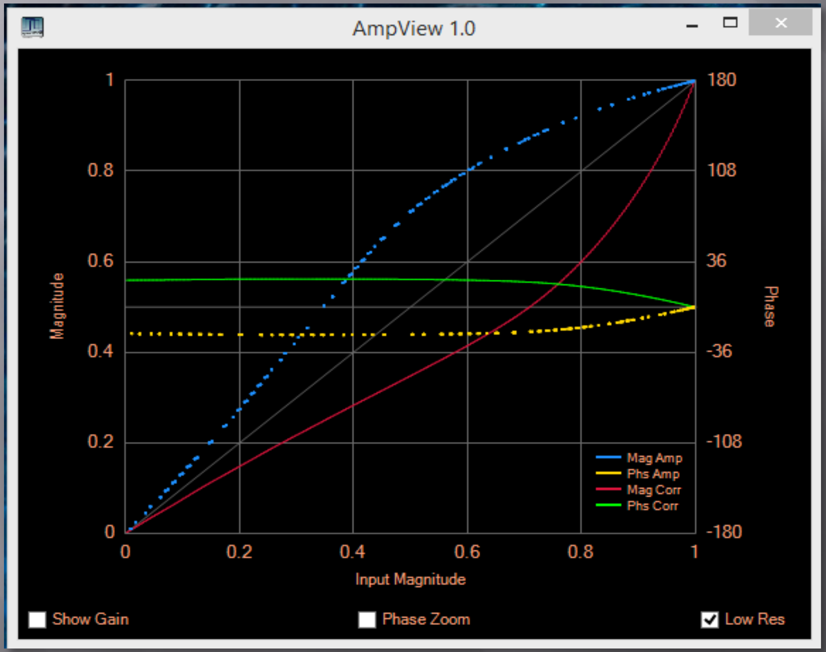
PURESIGNAL RESULTS
Clyde, K2UE

ANAN-100D

2M Xvtr

M² 2M-1K2

- ANAN Low-Pwr Xvtr Output
- Full-duplex Transverter
- 1200W 2M Amplifier



- 2M Amplifier is VERY non-linear
- LDMOS, Very low memory effects
- Should be very correctable!

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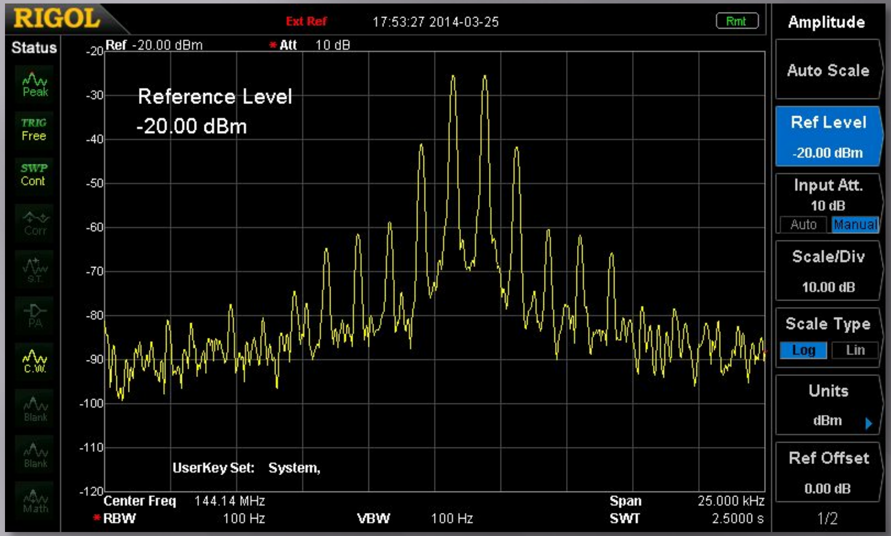
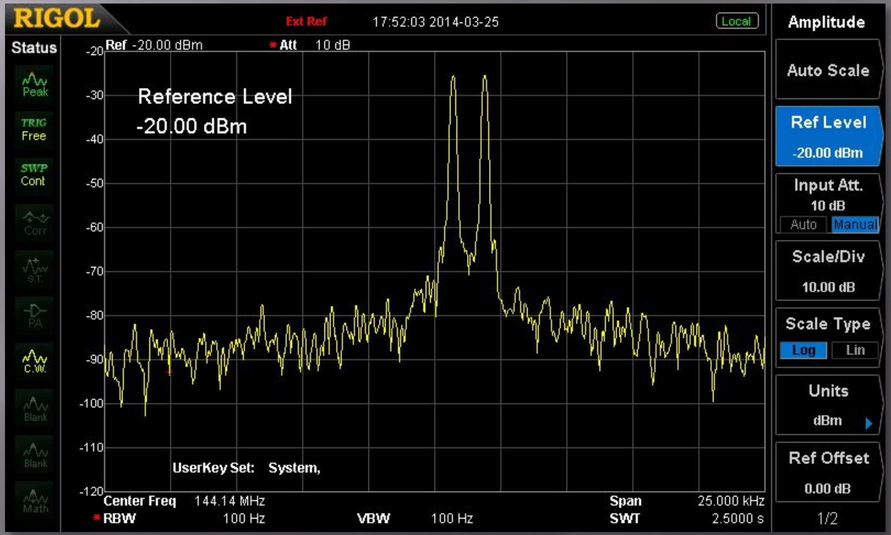
PURESIGNAL RESULTS

Clyde, K2UE



- PureSignal OFF
- IMD3 ~ -16dBt



- PureSignal ON
- IMD3 ~ -48dBt

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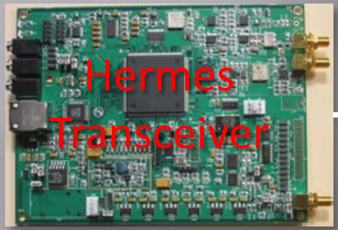
PURESIGNAL RESULTS

Focko, DJ5JB



Two P-P Stages
TI OPA2674C

2x RD16HHF1 MOSFET
2x MRF492 BJT

2x 3-500Z
(Grounded-grid)

MIXED TECHNOLOGY

- 80M, 900 Watts
- IMD3 -28 → -55 dBc
- IMD5 -34 → -70 dBc

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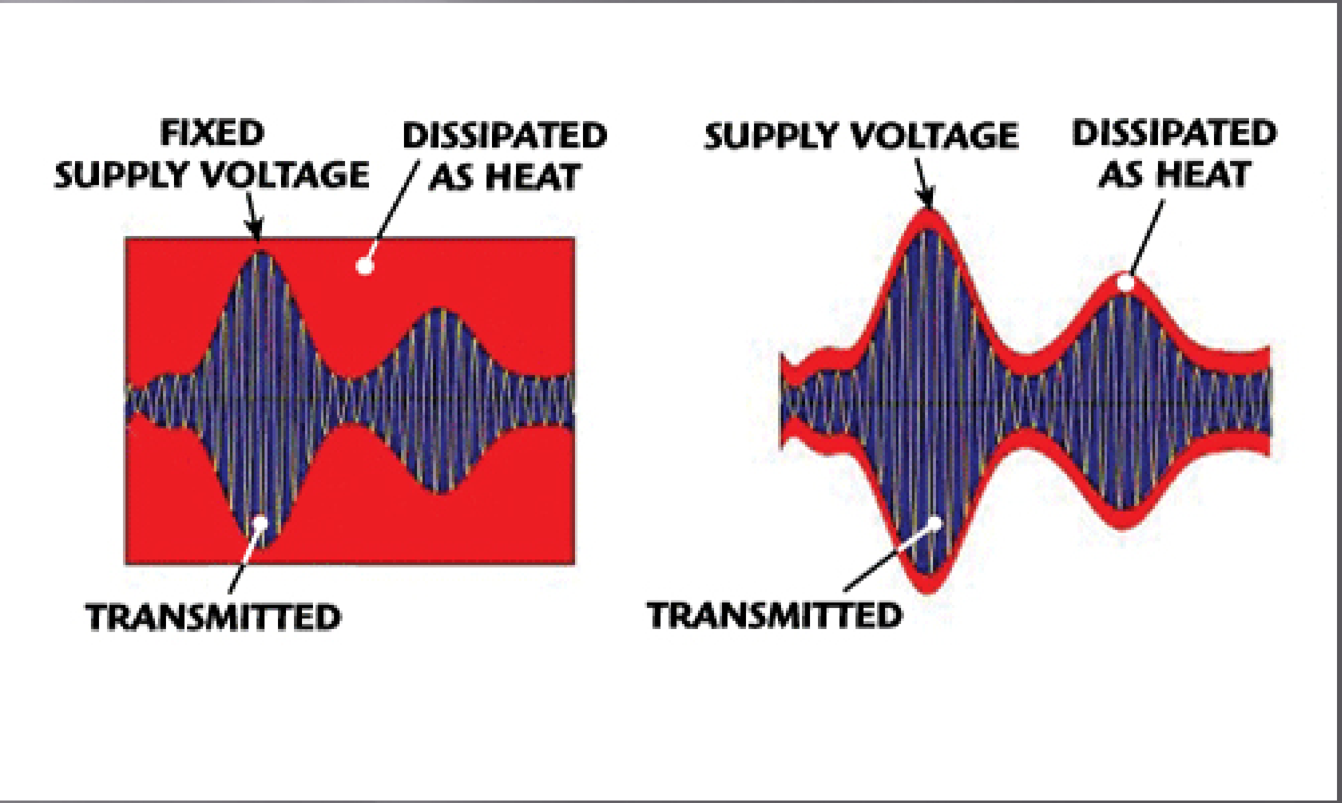
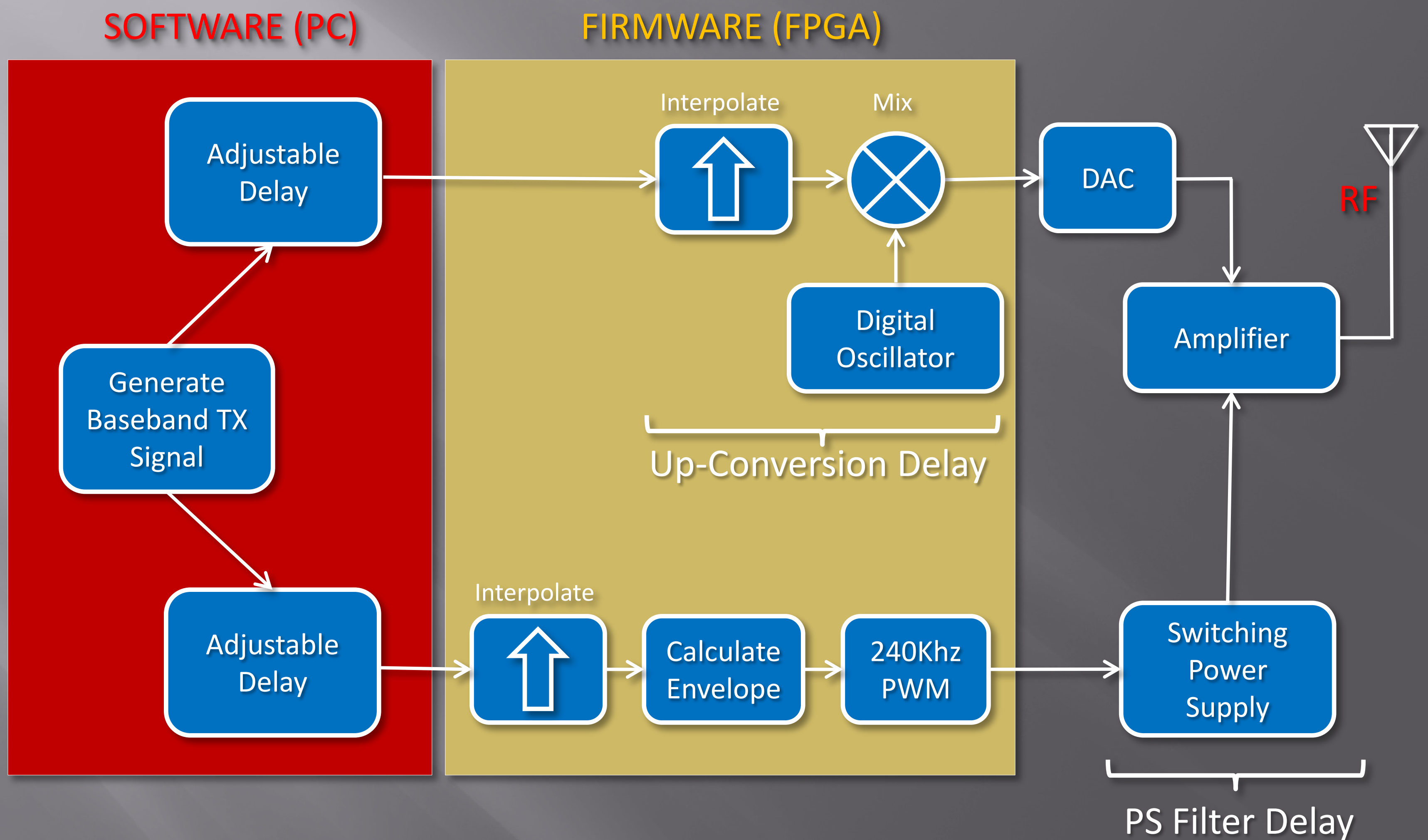
HIGHLY-EFFICIENT POWER AMPLIFIERS

EER (Envelope Elimination & Restoration)

ET (Envelope Tracking)



EER / ET IMPLEMENTATION



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NEW PROTOCOL FEATURES

- Each ADC can feed multiple DDCs.
  - Each DDC can output a different sample rate.
  - Completely independent DDCs.
- Multiple Synchronous DDCs
  - DDCs on separate ADCs can synchronously combine
- Multiple Synchronous DUCs
  - Beam forming
- DDC feeding DUC – linear translator

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NEW PROTOCOL FEATURES

- Based on *streams*
- Stream format defined when opened
- Standard stream types initially defined
- New stream types easy to define and add
- Use UDP port numbers to identify streams
- Port number assigned when stream opened

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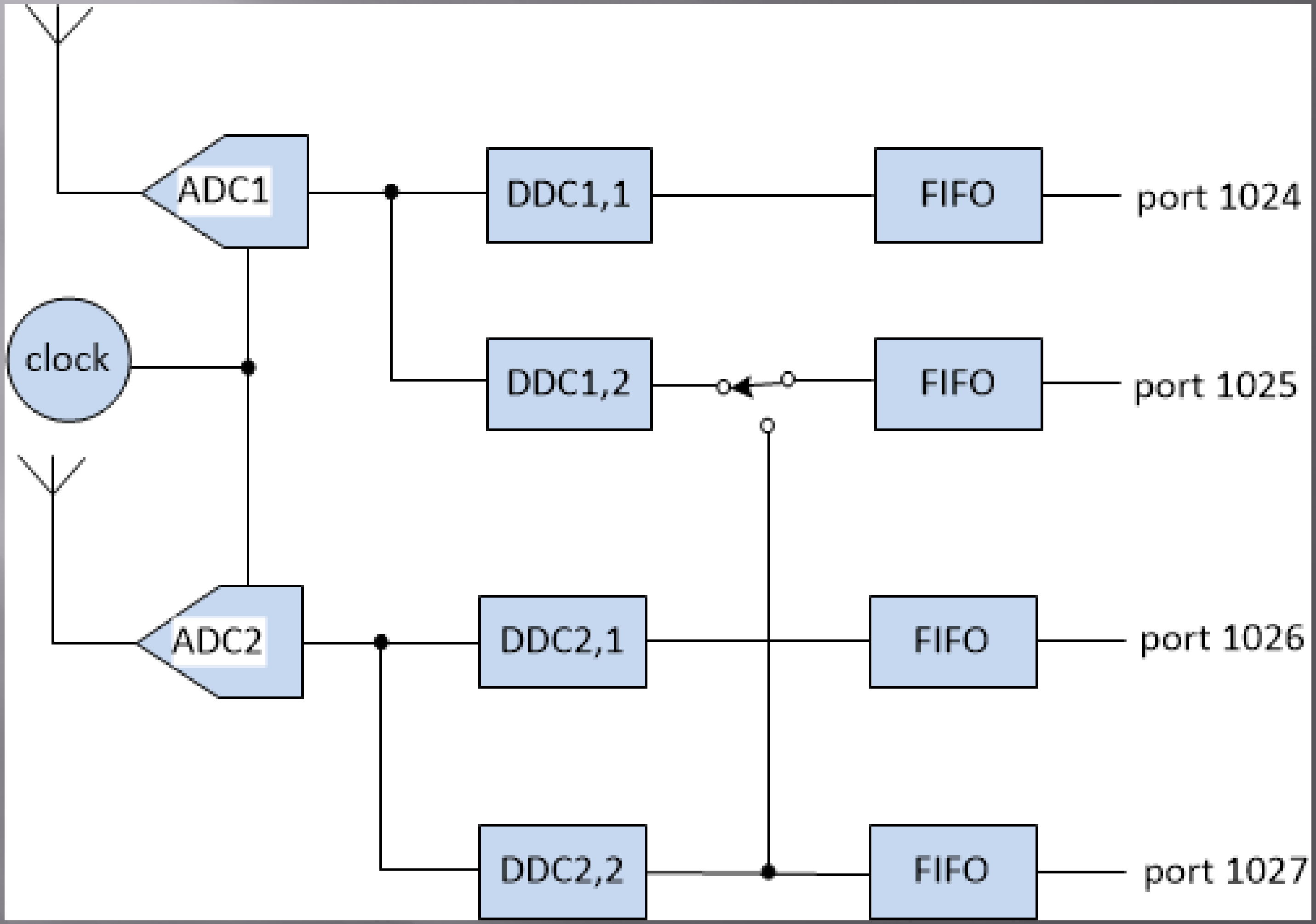
NEW PROTOCOL FEATURES



Credit – Phil Harman, VK6PH

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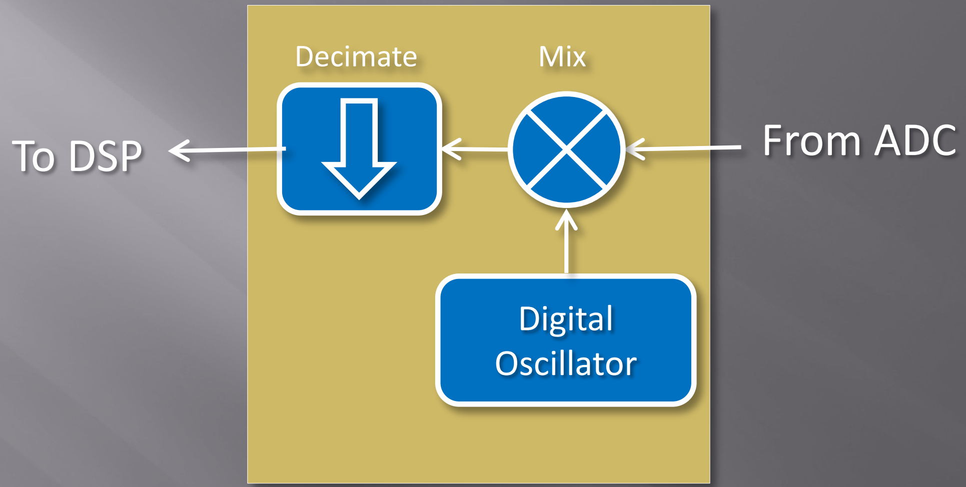
DIGITAL DOWN-CONVERSION
The Current Model



- Done in the time domain, in an FPGA
- Each DDC requires replicating the FPGA resources
- Each different frequency slice requires another DDC
- FPGA programming is less productive than software

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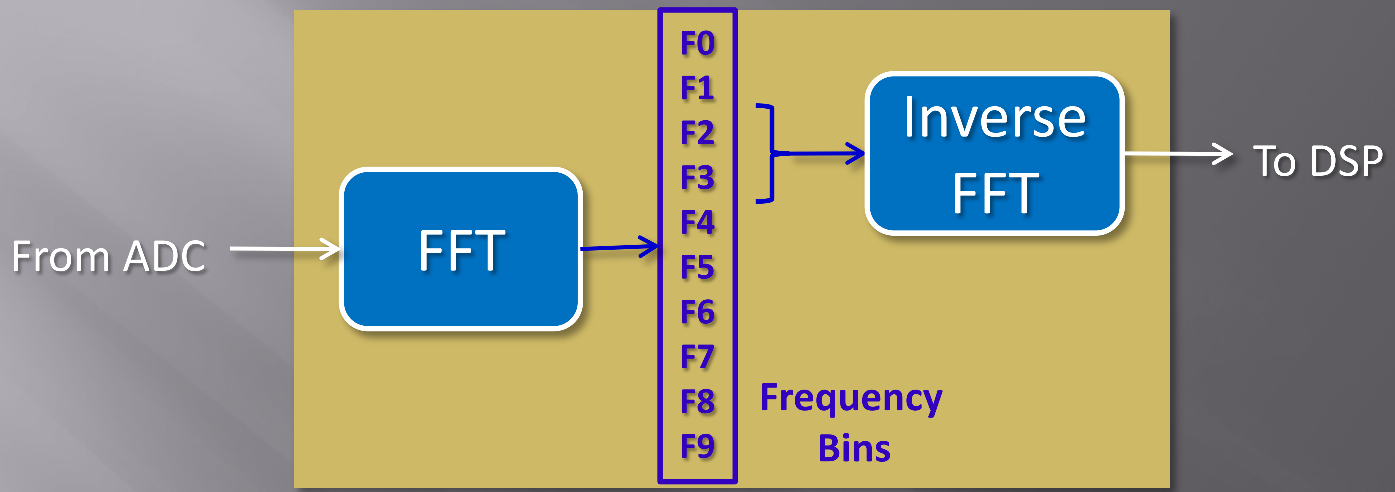
DIGITAL DOWN-CONVERSION
The DFC Model (Simplified !!)



- Done in the frequency domain, in an SBC or PC
- All DDCs use the same forward transform (the big one)
- Each different frequency slice requires an IFFT
- Programming is in software, e.g., in C

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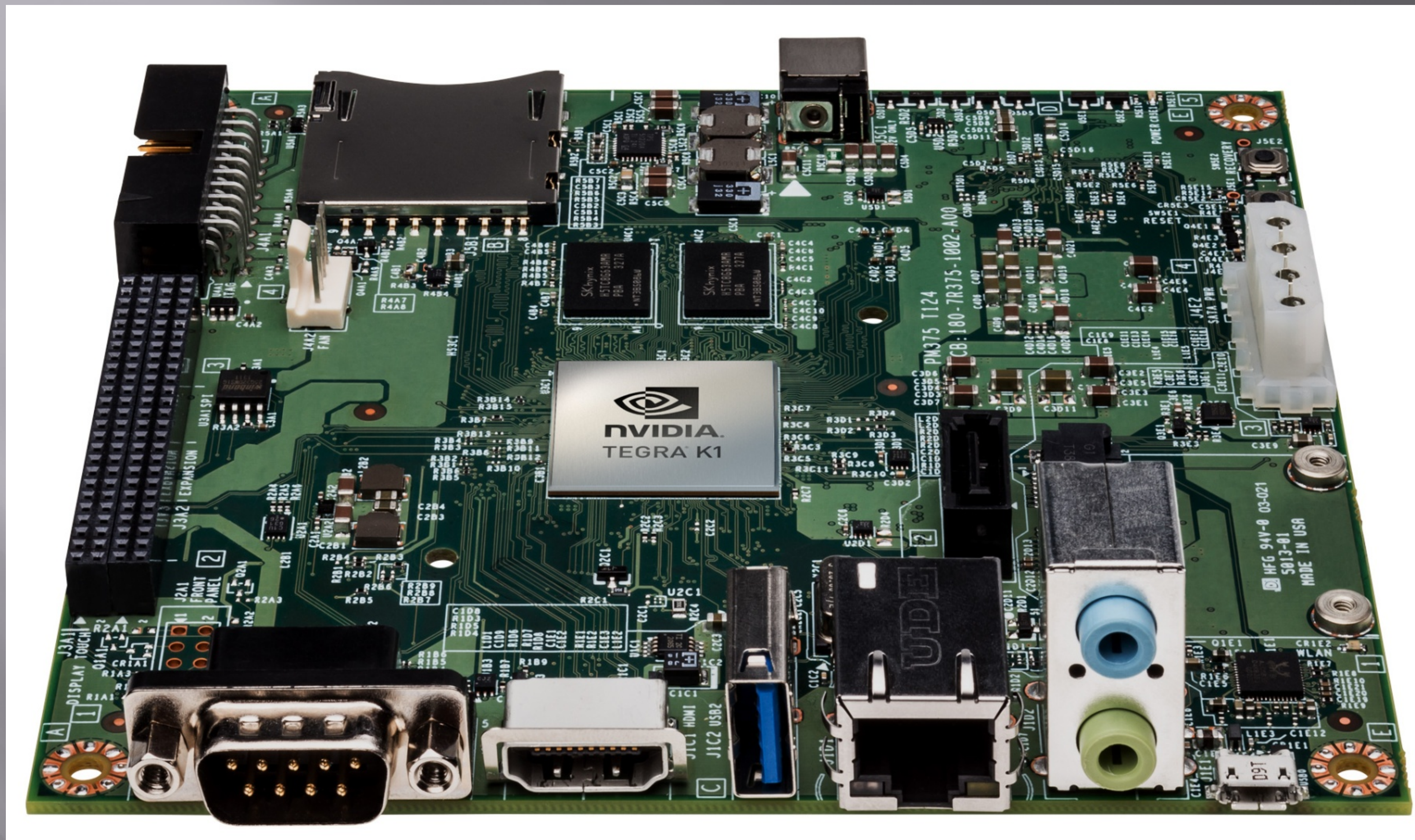
DIGITAL DOWN-CONVERSION
The DFC Model



Nvidia Jetson TK1: Quad-core ARM, 192 Cuda Cores, $ 192

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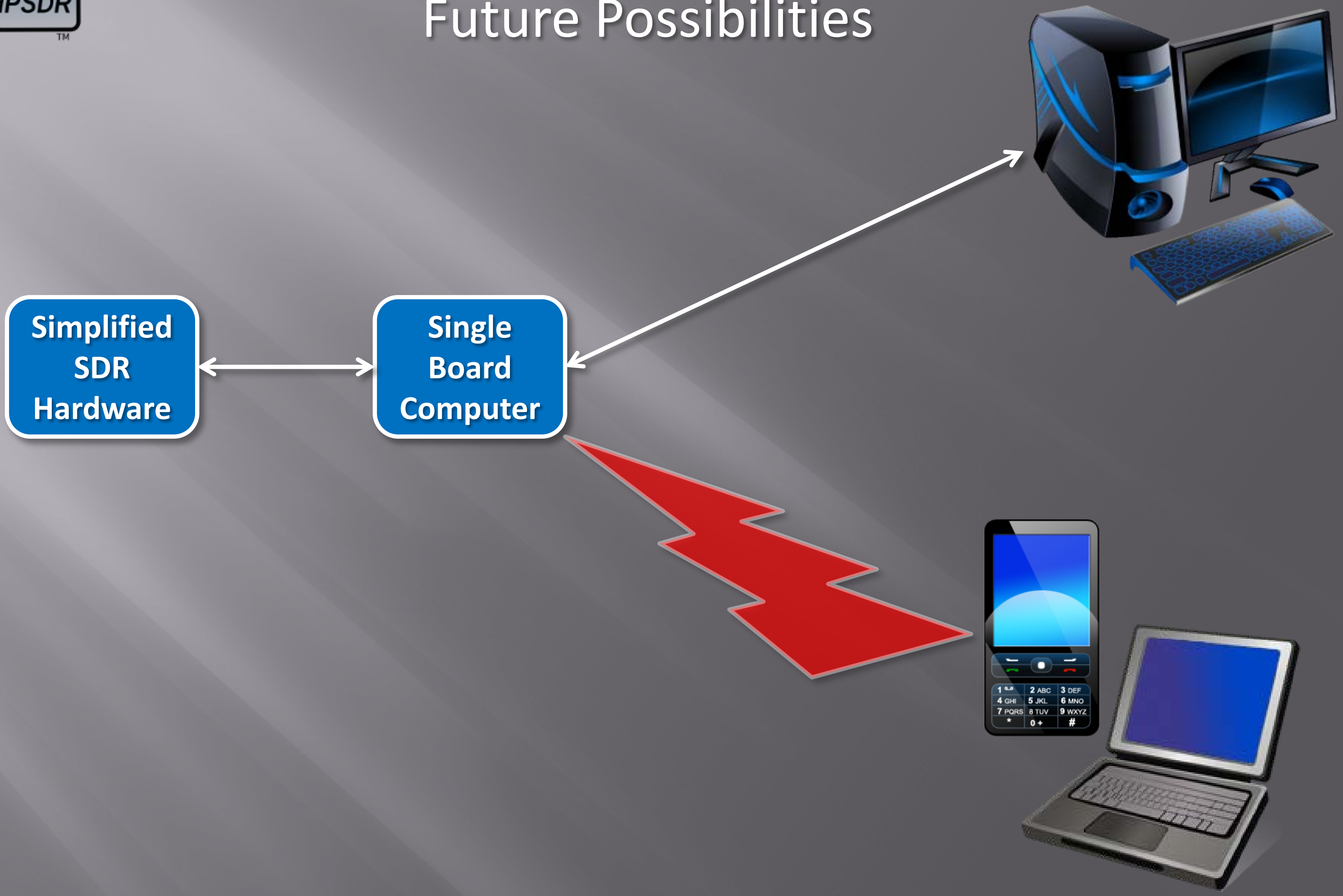
NEW ARCHITECTURE
Future Possibilities



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QUESTIONS?