**WHAT IS OpenHPSDR?**

**Open**
- An international group of SDR enthusiasts.

**High**
- Developing open-source hardware and software.

**Performance**
- Very “High Performance” designs --- extending the state of the art of SDR in Amateur Radio.

**Software**
- Having a lot of fun working with each other, challenging each other, and learning as we develop and test new technology.

**Defined**
- Partners (separate entities) include TAPR and Apache Labs.
OPENHPSDR TOPICS
PACIFICON 2014

NEW ITEMS THAT ARE NOW SHIPPING

• WDSP – New DSP library
• PureSignal – Adaptive pre-distortion
• EER / ET firmware & software

ACTIVE DEVELOPMENT

• New Communication Protocol

ACTIVE INVESTIGATION

• Direct Fourier Conversion & New Architectures
NEW ITEMS THAT ARE NOW SHIPPING

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WDSP

• Developed for our current and FUTURE openHPSDR needs

• Readily useable for other SDR projects

• Many enhanced and new functions

• Open-source, GNU GPL version 2

• C Programming Language – Close to the hardware & Efficient

• Shipping NOW! ( But, always opportunities to do more! 😊 )
THE CHANNEL CONCEPT

A software entity that accepts buffers of I,Q data and outputs buffers of I,Q data.
THE CHANNEL CONCEPT

The CHANNEL provides the home for a single UNIT such as a receiver or transmitter.
The UNIT comprises BLOCKS, each of which performs a specific function such as Filter, AM Modulator, or ALC.
• Each CHANNEL is completely independent of all others – Channels share nothing – No shared data or settings.
THE CHANNEL CONCEPT

• Each CHANNEL is completely independent of all others – Channels share nothing – No shared data or settings.

• You can have as many channels as you want.
THE CHANNEL CONCEPT

- Each CHANNEL is completely independent of all others – Channels share NOTHING – No shared data or settings.
- You can have as many channels as you want.
- The CHANNEL structure is always exactly the same, no matter what type of unit is housed within it.
THE CHANNEL CONCEPT

• After defining a UNIT, you can use that definition within as many channels as you want.

• Pre-defined units include a Receiver & a Transmitter.

• It is simple to add new types of units – very uniform structure to “splice” them into channels.
THE CHANNEL CONCEPT

- After defining a BLOCK, you can use that definition as many times as you want within a single unit and you can use that definition in other units.
- BLOCKS also have a very uniform structure.
Single CHANNEL structure, uniform UNIT structure, and uniform BLOCK structure support easy re-use of technology and more rapid development.
A rich assortment of BLOCKs has been included!
WDSP
AVAILABLE BLOCKS

• Frequency-shifter (complex oscillator + mixer)
• Resampler
• Signal Generators
  • sine, pulse, two-tone, triangle, noise, sawtooth
• Adjustable bandpass filters
• AM squelch & transmit noise-gate
  • raised-cosine transitions
  • continuously variable tail length
• AM Demodulation
  • basic & synchronous modes
  • sideband selection (lower, upper, or both) – true phasing separation, not filtering
  • carrier stabilization
WDSP
AVAILABLE BLOCKS

• FM Demodulation
  • de-emphasis
  • CTCSS block
• FM Squelch
  • raised-cosine transitions
  • continuously variable tail length
• Equalizer
  • continuous-gain (as opposed to gain by band)
  • specify gain at any number of frequencies
• Automatic Notch Filter (LMS algorithm)
  • automatic variable leak
• Automatic Noise Reduction (LMS algorithm)
  • automatic variable leak
WDSP
AVAILABLE BLOCKS

• Speech processor
  • characteristics of an RF speech processor
• AM modulator
  • zero carrier shift
  • absolute 100% modulation control available
• FM modulator
  • pre-emphasis (either before or after limiting)
  • CTCSS tones
• Preemptive NoiseBlanker
  • slew time, advance time, hang time control
• Diversity mixing
• PureSignal transmit linearity correction
• Audio Peaking Filters for CW & RTTY

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WDSP
AVAILABLE BLOCKS

• AGC / ALC / Audio Leveler
  • ZERO overshoot (total amplitude control)
  • automatic fast decay mode for transients
  • hang functionality
  • slope functionality (strong stations sound louder)
  • get / set functions for controls on panadapter

• Patchpanel
  • select I or Q or I and Q
  • copy I → Q or Q → I
  • mutual and separate I, Q gain controls
  • use for input select, audio pan, binaural output selection, etc.
WDSP
AVAILABLE BLOCKS

• Meters
  • peak, average, and gain modes
• Phase & scope display
• Panadapter / Spectrum display
  • large FFT support for weak signal
  • stitched spectra for wider display
  • adjustable frame rate (independent of sample rate and FFT size)
• spur elimination for Cyclops spectrum analyzer
• resamples to chosen pixel width
• selection of window functions
• selection of averaging modes
• AND MORE ...
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ACTIVE DEVELOPMENT

• New Communication Protocol

ACTIVE INVESTIGATION

• Direct Fourier Conversion & New Architectures
• Mix With Complex Oscillator To Generate Baseband (0 Hz IF) Signal
• Decimate Down From The Sample Rate Of The Oscillator & ADC (122.88 Mhz)

• Process The Complex Digital Signal (I,Q) To Generate Audio
  • Sample rates are easily processed in software (48K – 384K)
• Complex Digital Signal (I,Q) Generated From Audio Data
  • Sample rates are easily processed in software (48K – 384K)

• Interpolate Up To The Sample Rate Of The DAC & Oscillator (122.88 Mhz)
• Mix With Complex Oscillator To Generate The RF-Frequency Digital Signal
DDC / DUC
Since 2006

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DUC TRANSMITTER

GENERATE DIGITAL SIGNAL

MIC → ADC → Process in Software DSP → Digital Signal Generator

DIGITAL UPCONVERSION

Interpolate → Mix → DAC → Amplifier

Digital Oscillator
DUC TRANSMITTER

**GENERATE DIGITAL SIGNAL**

- MIC
- ADC
- Process in Software DSP
- Digital Signal Generator

**DIGITAL UPCONVERSION**

- Interpolate
- Mix
- Digital Oscillator
- DAC
- Amplifier

- RF

**Graph:**

- Frequency range: 14.180 to 14.220
- Signal levels: -20 to -140 dBm

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DUC TRANSMITTER

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**DIGITAL UPCONVERSION**

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- Mix
- Digital Oscillator
- DAC
- Amplifier
- RF
**DUC TRANSMITTER**

**GENERATE DIGITAL SIGNAL**
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**DUC TRANSMITTER**

**GENERATE DIGITAL SIGNAL**
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**DIGITAL UPCONVERSION**
- Interpolate → Mix → DAC → Amplifier → RF
- Digital Oscillator

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DUC TRANSMITTER

Generate Digital Signal

MIC → ADC → Process in Software DSP → Digital Signal Generator

Digital Signal Generator

Digital Oscillator

Interpolate → Mix → DAC → Amplifier → RF

Digital Upconversion


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WHY ?
WHY?

Because the amplifier is NOT perfectly linear!
AMPLITUDE NON-LINEARITY

![Graph showing Amplifier Input vs Amplifier Output with Ideal and Actual lines]

- **Amplifier Input**
- **Amplifier Output**

- Blue line represents **Ideal**
- Red line represents **Actual**

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CORRECT BY PREDISTORTION

Amplifier Input

Amplifier Output

Ideal
Actual
PD Input

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ADAPTIVE BASEBAND PREDISTORTION

Basic Concept

- Apply Correction to the out-bound signal
- Calculate Correction by Comparing the Input & Output of the Amplifier
  - BASEBAND – I,Q Before Up-Conversion / I,Q After Down-Conversion
  - ADAPTIVE – Repeat the process to Adapt to Changing Conditions
PURESIGNAL RESULTS
Clyde, K2UE

ANAN-100D • ANAN Low-Pwr Xvtr Output
2M Xvtr • Full-duplex Transverter
M² 2M-1K2 • 1200W 2M Amplifier

- 2M Amplifier is VERY non-linear
- LDMOS, Very low memory effects
- Should be very correctable!
PURESIGNAL RESULTS
Clyde, K2UE

- PureSignal OFF
- IMD3 ~ -16dBt

- PureSignal ON
- IMD3 ~ -48dBt
PURESIGNAL RESULTS
Focko, DJ5JB

Hermes Transceiver
Two P-P Stages
TI OPA2674C

Hercules 100W PA (DIBAY)
2x RD16HHF1 MOSFET
2x MRF492 BJT

LK-500 NTC
2x 3-500Z (Grounded-grid)

MIXED TECHNOLOGY
- 80M, 900 Watts
- IMD3 -28 → -55 dBc
- IMD5 -34 → -70 dBc

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ACTIVE DEVELOPMENT

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ACTIVE INVESTIGATION

• Direct Fourier Conversion & New Architectures
HIGHLY-EFFICIENT POWER AMPLIFIERS

EER (Envelope Elimination & Restoration)
ET (Envelope Tracking)
EER / ET IMPLEMENTATION

SOFTWARE (PC)

- Adjustable Delay
- Generate Baseband TX Signal
- Adjustable Delay

FIRMWARE (FPGA)

- Interpolate
- Mix
- Interpolate
- Calculate Envelope
- 240Khz PWM
- Interpolate
- Digital Oscillator
- DAC
- Up-Conversion Delay
- Amplifier
- Switching Power Supply
- PS Filter Delay

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PACIFICON  2014

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NEW PROTOCOL FEATURES

• Each ADC can feed multiple DDCs.
  • Each DDC can output a different sample rate.
  • Completely independent DDCs.

• Multiple Synchronous DDCs
  • DDCs on separate ADCs can synchronously combine

• Multiple Synchronous DUCs
  • Beam forming

• DDC feeding DUC – linear translator

Credit – Phil Harman, VK6PH
NEW PROTOCOL FEATURES

• Based on *streams*

• Stream format defined when opened

• Standard stream types initially defined

• New stream types easy to define and add

• Use UDP port numbers to identify streams

• Port number assigned when stream opened

Credit – Phil Harman, VK6PH
NEW PROTOCOL FEATURES

Credit – Phil Harman, VK6PH
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ACTIVE DEVELOPMENT

- New Communication Protocol

ACTIVE INVESTIGATION

- Direct Fourier Conversion & New Architectures
• Done in the time domain, in an FPGA
• Each DDC requires replicating the FPGA resources
• Each different frequency slice requires another DDC
• FPGA programming is less productive than software
DIGITAL DOWN-CONVERSION
The DFC Model (Simplified !!)

- Done in the frequency domain, in an SBC or PC
- All DDCs use the same forward transform (the big one)
- Each different frequency slice requires an IFFT
- Programming is in software, e.g., in C
DIGITAL DOWN-CONVERSION
The DFC Model

Nvidia Jetson TK1: Quad-core ARM, 192 Cuda Cores, $192
NEW ARCHITECTURE
Future Possibilities

- Simplified SDR Hardware
- Single Board Computer
QUESTIONS?