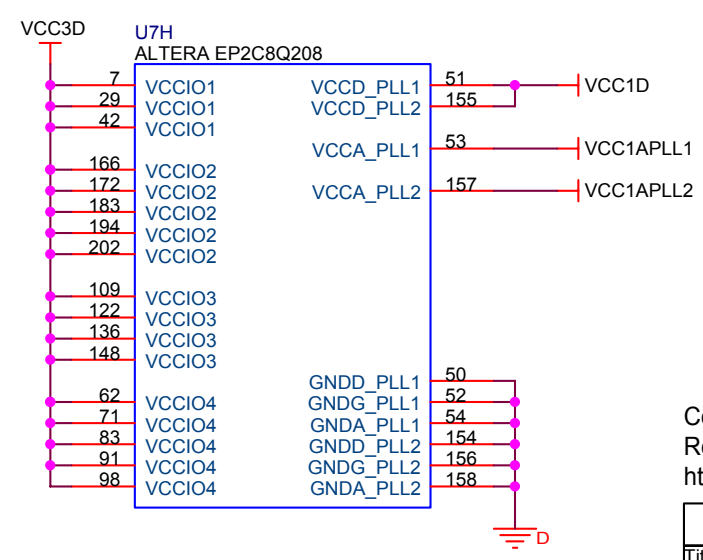
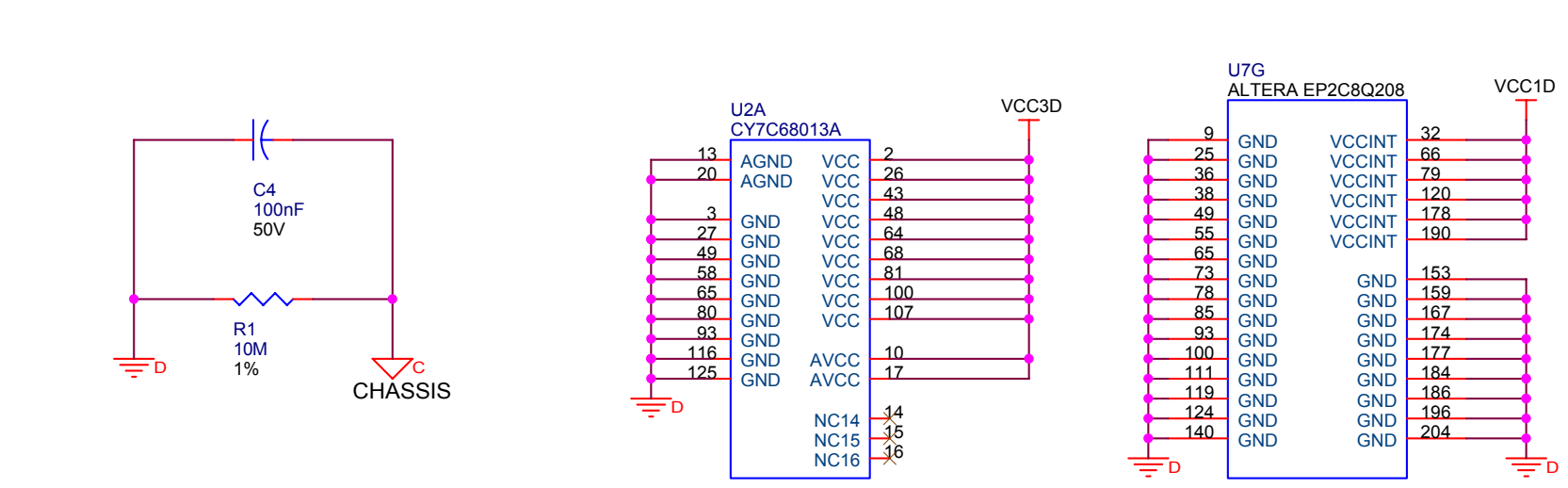


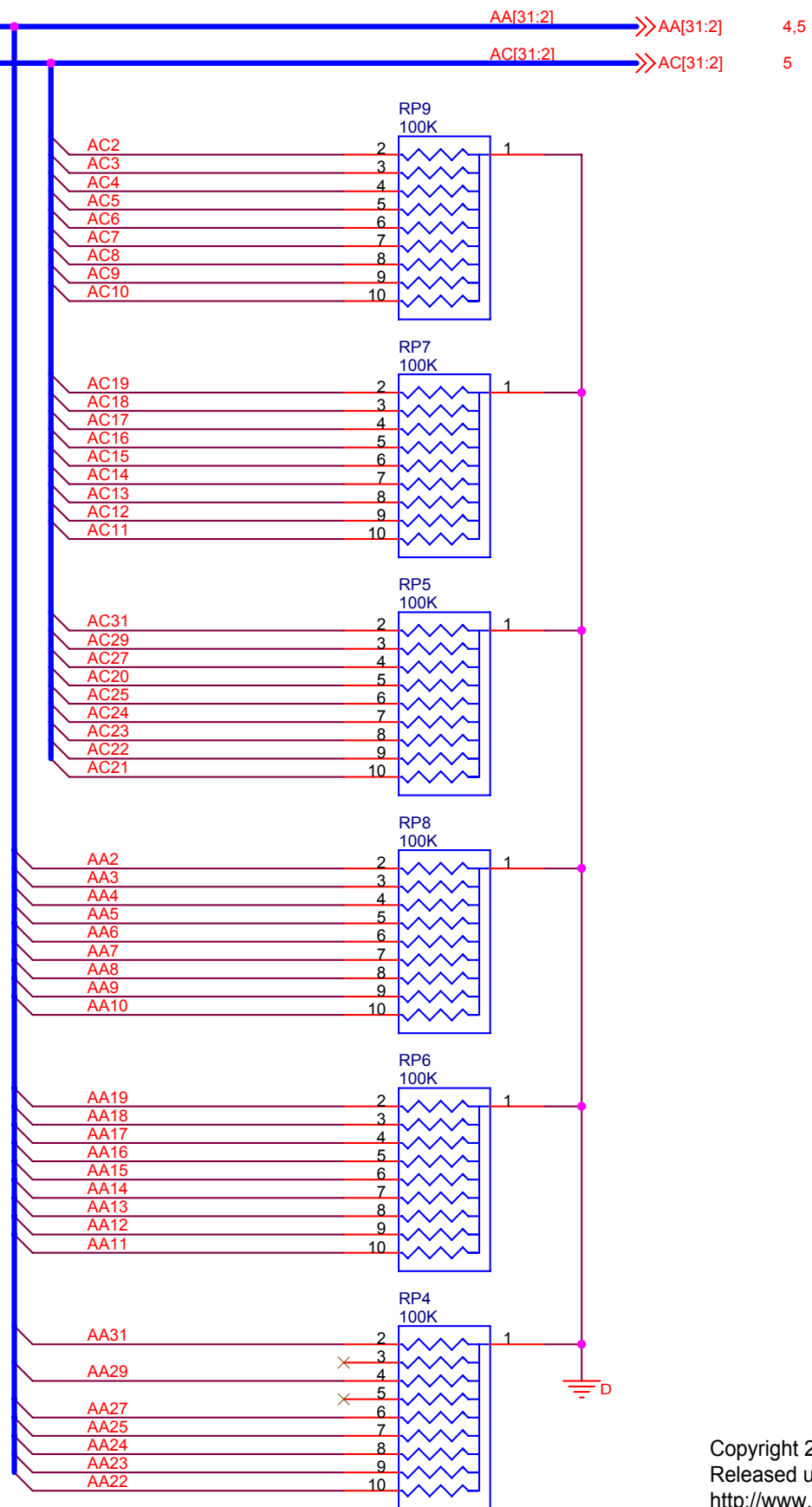
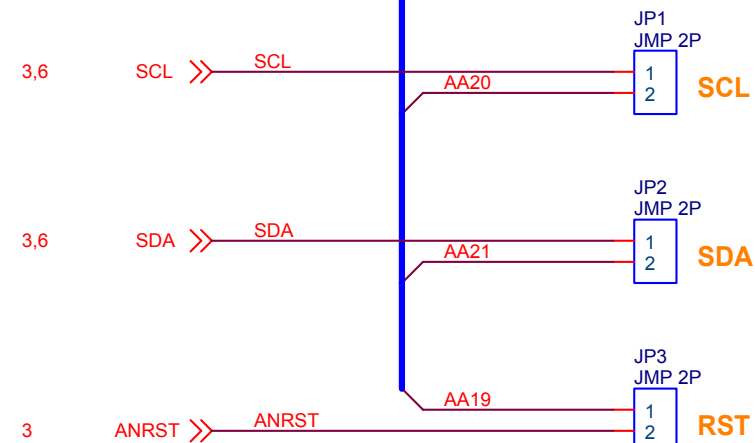
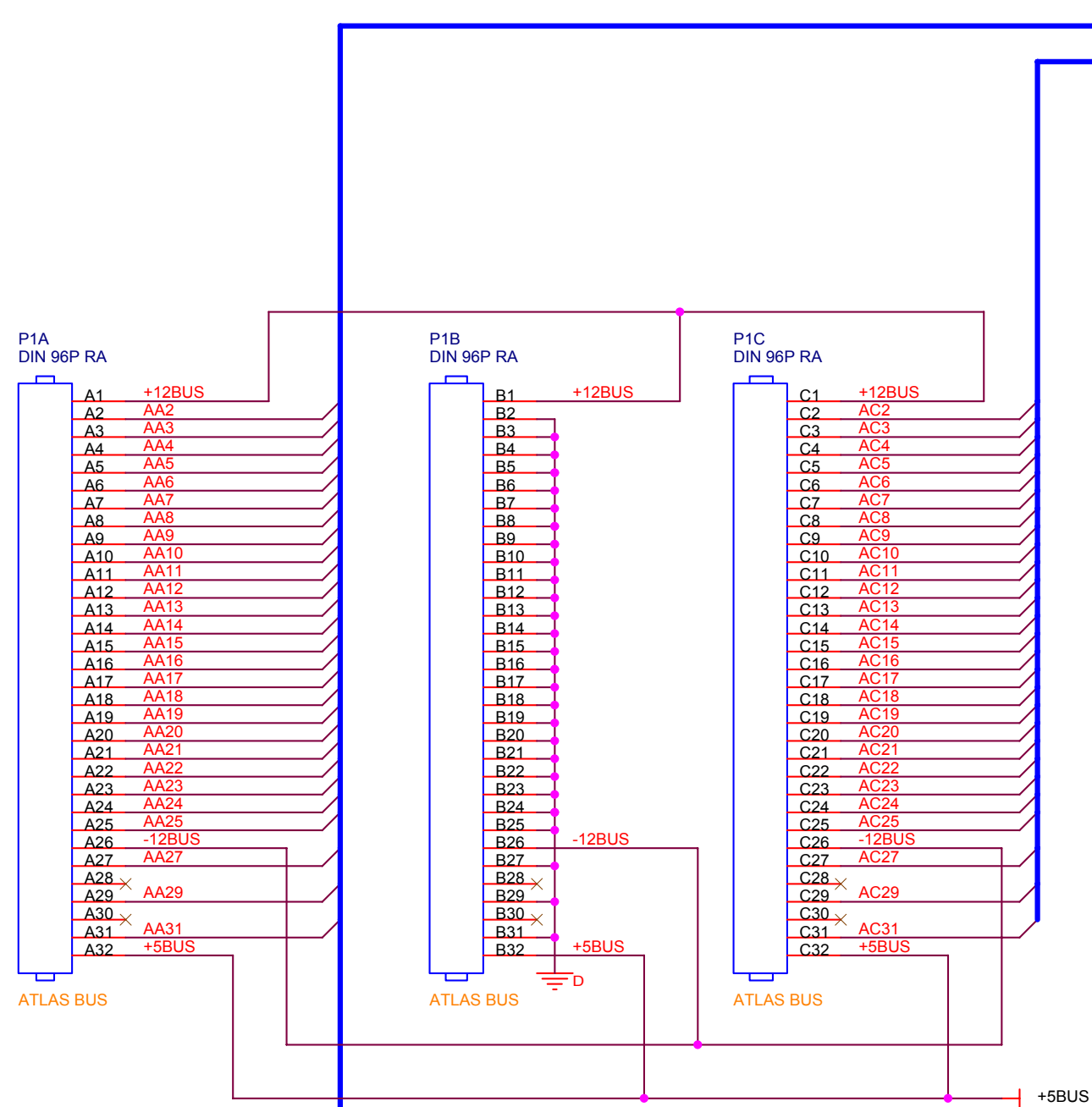
Revision History

Date	Revision	By	Description
22 Aug 2009	XA6	WA2DFI	Reformatted from Lyle's schematic, added properties
26 Aug 2009	XA7	KK7P	Changed connections of D10, D11; Q1, Q2 to 2N7002K (Sheet 5).



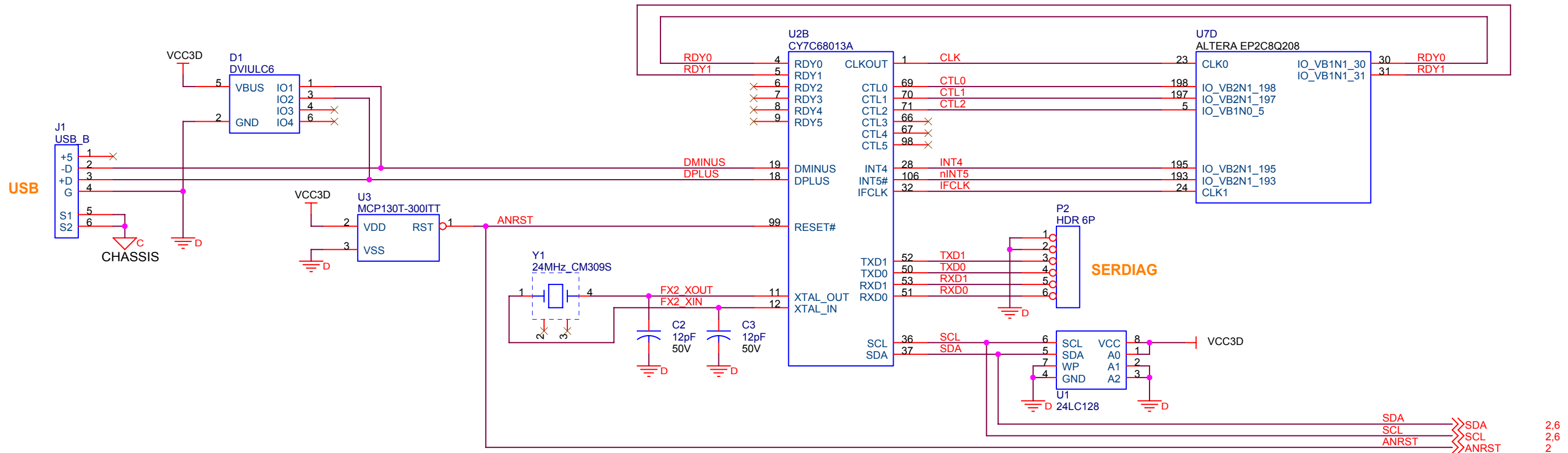
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Title		
HPSDR Magister: Bypass and Power		
Size	Document Number	Rev
B	2009071901	XA7
Date:	Wednesday, August 26, 2009	Sheet 1 of 6



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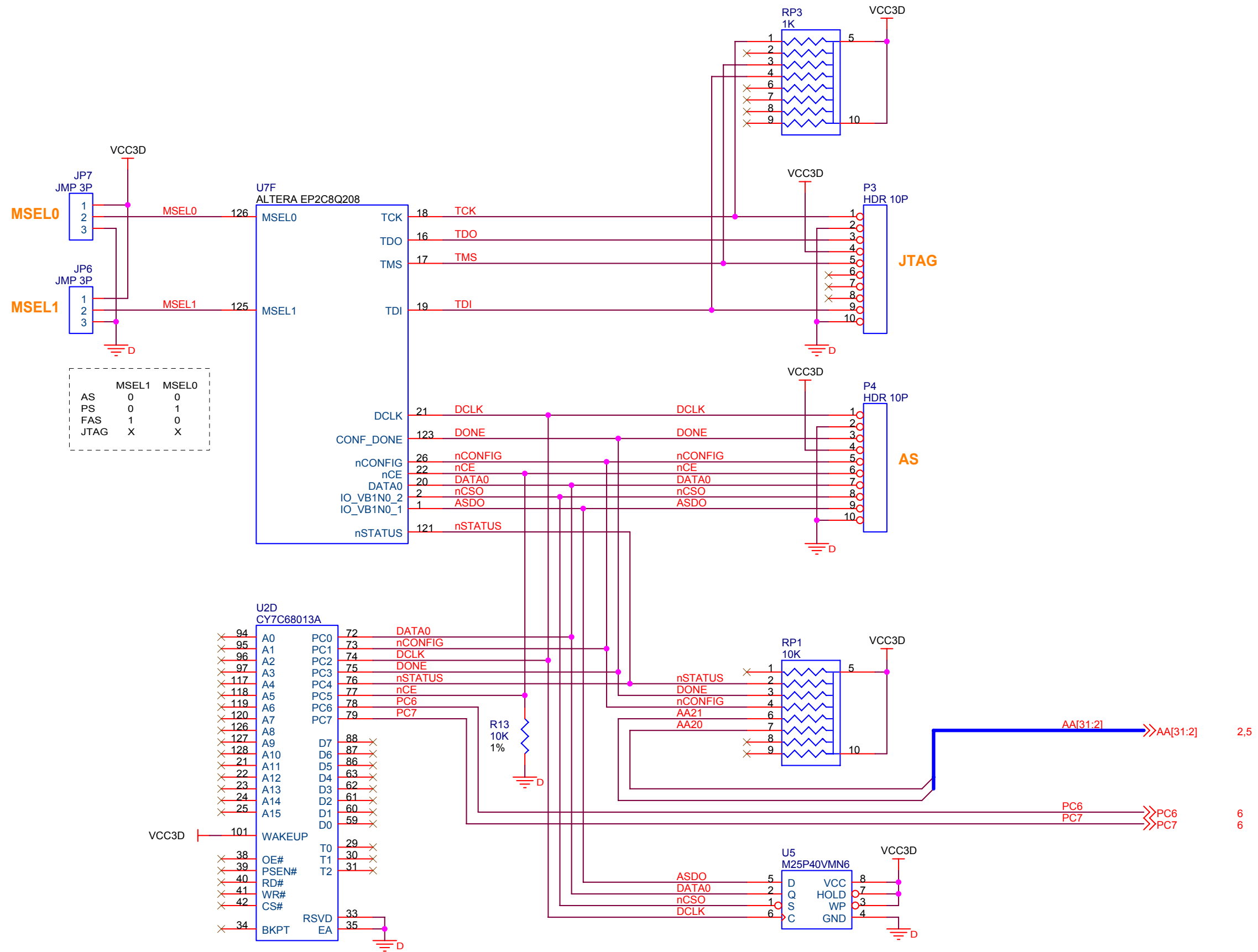
Title		
HPSDR Magister: Bus Interface		
Size	Document Number	Rev
B	2009071901	XA7
Date:	Thursday, August 27, 2009	Sheet 2 of 6



U7A ALTERA EP2C8Q208				U2C CY7C68013A				U7B ALTERA EP2C8Q208			
67	VREFB4N1	IO_VB1N0_15	15	PA0	82	PA0	PB0	44	PB0	56	DEV_OE
68	IO_VB4N1_68	IO_VB1N0_14	14	PA1	83	PA1	PB1	45	PB1	57	IO_VB4N1_57
69	IO_VB4N1_69	VREFB1N0	13	PA2	84	PA2	PB2	46	PB2	58	IO_VB4N1_58
70	IO_VB4N1_70	IO_VB1N0_12	12	PA3	85	PA3	PB3	47	PB3	59	IO_VB4N1_59
72	IO_VB4N1_72	IO_VB1N0_11	11	PA4	89	PA4	PB4	54	PB4	60	IO_VB4N1_60
74	IO_VB4N1_74	IO_VB1N0_10	10	PA5	90	PA5	PB5	55	PB5	61	IO_VB4N1_61
75	IO_VB4N1_75	IO_VB1N0_8	8	PA6	91	PA6	PB6	56	PB6	63	IO_VB4N1_63
76	IO_VB4N0_76	IO_VB1N0_6	6	PA7	92	PA7	PB7	57	PB7	64	IO_VB4N1_64
77	IO_VB4N0_77										
80	IO_VB4N0_80	IO_VB1N1_35	35	PE0	108	PE0	PD0	102	PD0	208	IO_VB2N1_208
81	IO_VB4N0_81	VREFB1N1	37	PE1	109	PE1	PD1	103	PD1	207	IO_VB2N1_207
82	IO_VB4N0_82	IO_VB1N1_39	39	PE2	110	PE2	PD2	104	PD2	206	DEV_CLRn
89	VREFB4N0	IO_VB1N1_40	40	PE3	111	PE3	PD3	105	PD3	205	IO_VB2N1_205
90	IO_VB4N0_90	IO_VB1N1_41	41	PE4	112	PE4	PD4	121	PD4	203	IO_VB2N1_203
92	IO_VB4N0_92	IO_VB1N1_43	43	PE5	113	PE5	PD5	122	PD5	201	IO_VB2N1_201
94	IO_VB4N0_94	IO_VB1N1_44	44	PE6	114	PE6	PD6	123	PD6	200	IO_VB2N1_200
95	IO_VB4N0_95	IO_VB1N1_45	45	PE7	115	PE7	PD7	124	PD7	199	IO_VB2N1_199
129	CLK7										
130	CLK6										
131	CLK5										
132	CLK4										

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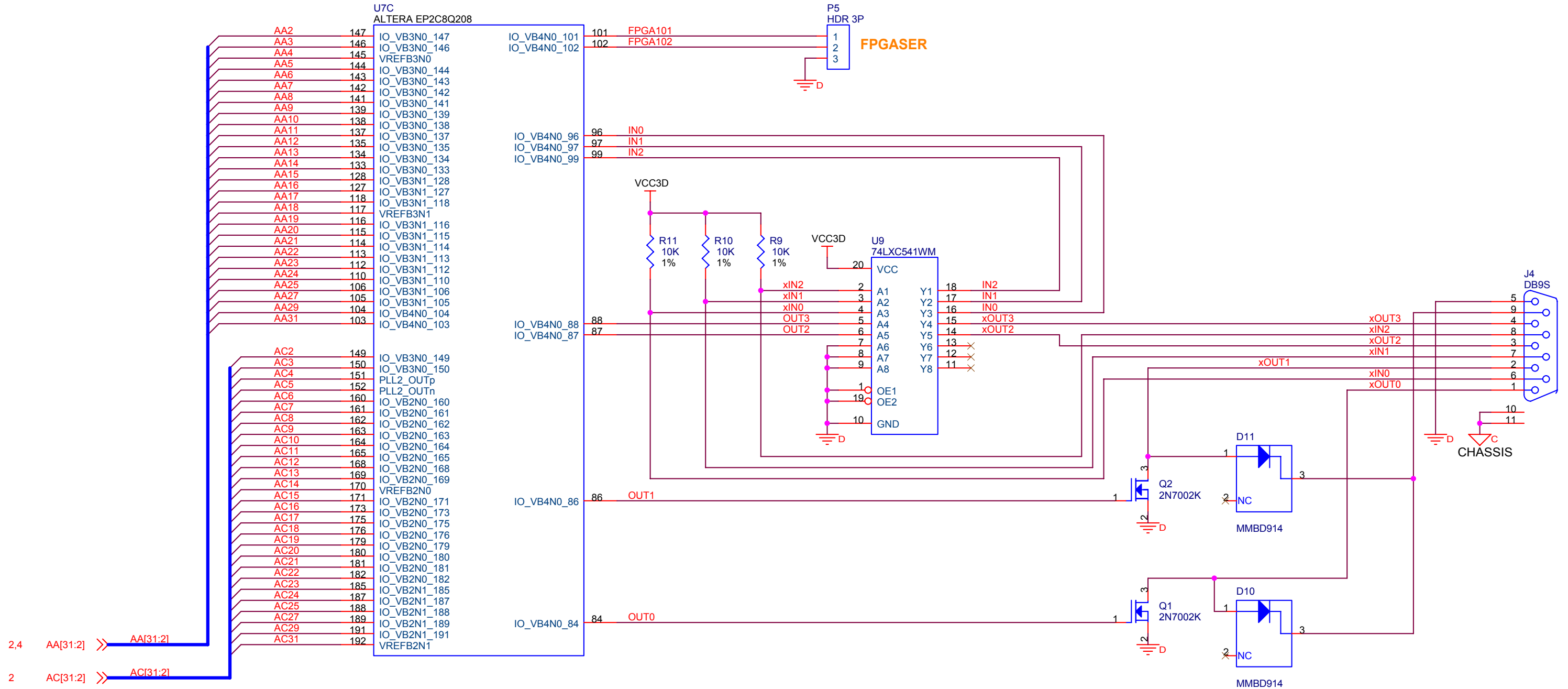
Title HPSDR Magister: FX2		
Size B	Document Number 2009071901	Rev XA7
Date: Thursday, August 27, 2009	Sheet 3	of 6



	MSEL1	MSEL0
AS	0	0
PS	0	1
FAS	1	0
JTAG	X	X

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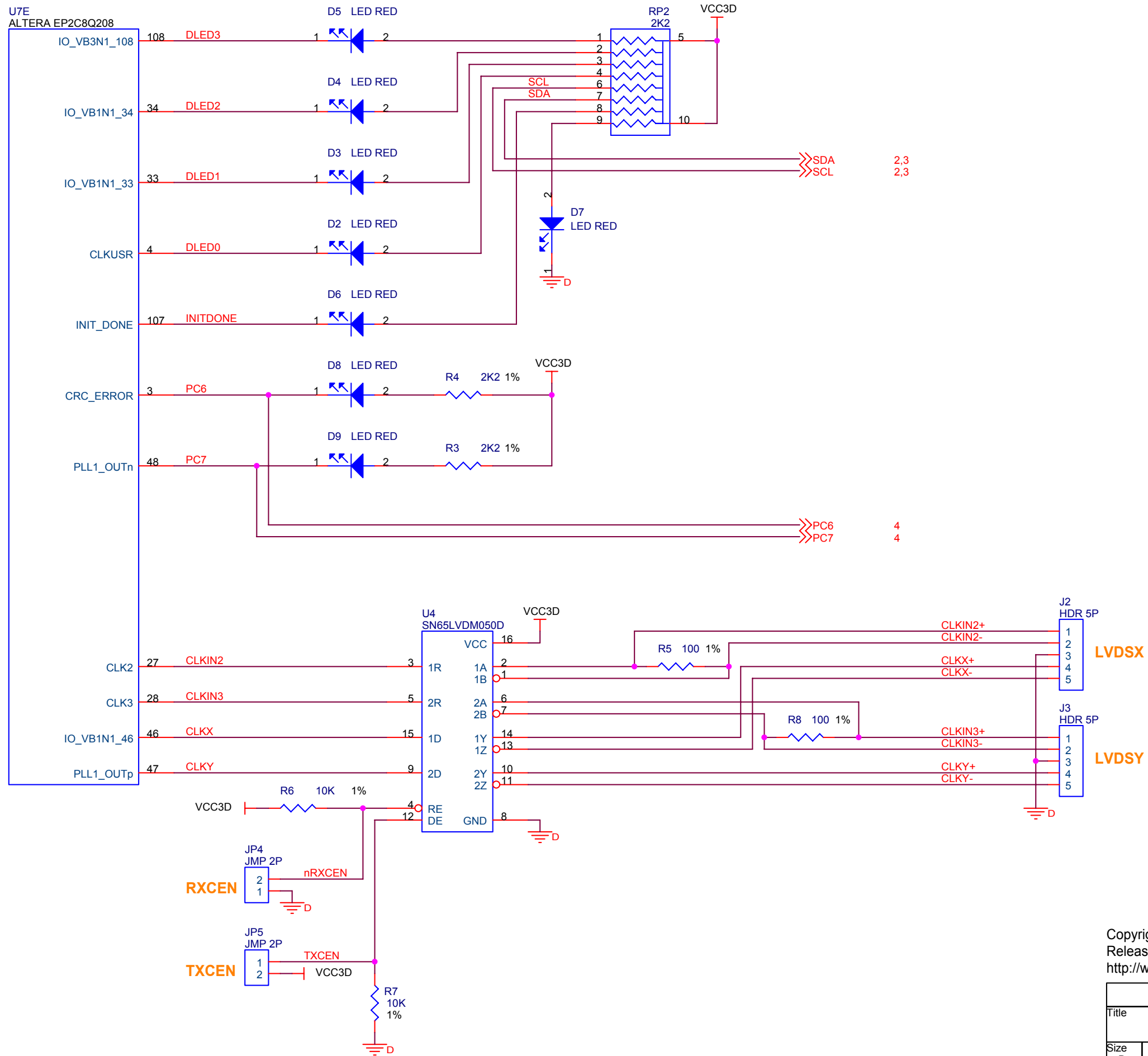
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HPSDR Magister: FPGA Configuration		
Size	Document Number	Rev
B	2009071901	XA7
Date:	Wednesday, August 26, 2009	Sheet 4 of 6



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 2 AC[31:2] >> AC[31:2]

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Title		
HPSDR Magister: FPGA		
Size	Document Number	Rev
B	2009071901	XA7
Date:	Wednesday, August 26, 2009	Sheet 5 of 6



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Title		
HPSDR Magister: LEDs and I/O		
Size	Document Number	Rev
B	2009071901	XA7
Date:	Wednesday, August 26, 2009	Sheet 6 of 6