Magister/Ozy differences  
v 1.0 – 5 Oct 2009 WA2DFI

1. **Power Supply source**

Jumpers J32 and J26 allowed Ozy to be powered from the Atlas bus 5VDC rail, the USB cable or the Atlas bus 3.3VDC rail. The TAPR manufactured Ozy default was powered from the Atlas 5VDC rail. These jumpers are removed on Magister, which is always powered from the Atlas 5VDC rail.

2. **Zero-ohm resistors have been replaced with headers for push-on jumpers**

Ozy J27 and J28 zero-ohm resistors were used to connect/disconnect the I2C PROM to Atlas bus pins A20 and A21. These have been replaced with Magister JP1 and JP2 headers.

Ozy J29 zero-ohm resistor was used to optionally connect the POR chip to Atlas bus pin A19. It has been replaced with header JP3 on Magister.

Ozy J23 and J24 zero-ohm resistors were used to select the FPGA load mode. These have been replaced with Magister JP6 and JP7 headers.

Ozy J12 and J13 zero-ohm resistors were used to enable the LVDS drivers and receivers. These have been replaced with Magister JP4 and JP5 headers.

3. **Some Ozy headers have been removed**

Ozy headers J5 (I2C EXT) and J7 (EXT RESET) have been removed.

Ozy header J21 (EXTERNAL CLOCKS) has been removed.

4. **The 1-wire bus interface on Atlas bus pin A18 has been removed**

It never worked anyway, as the DS2480B (Ozy U2) part is a 5V part connected to 3.3V.

5. **The RS-232 level converter has been removed**

Ozy RS-232 level converter (U7) has been removed. All three serial ports (two from the FX2, one from the FPGA) now connect directly to headers. On Ozy, one serial port was connected to the 1-wire interface and the other was level converted and connected to header J6. On Magister, both of these ports go directly to header P2 with no level conversion. On Ozy, two pins of the FPGA were level converted and connected to header J6 for use as a serial port. On Magister, the same two FPGA go directly to header P5 with no level conversion.
6. **Optional crystal oscillators have been removed**

   Ozy optional oscillators Y2 and Y3 have been removed, along with their associated zero-ohm jumpers J10 and J11.

7. **LVDS clock headers have been combined**

   Ozy LVDS I/O headers J2 and J3 have been replaced with a combined header, Magister J2. Ozy LVDS I/O headers J1 and J4 have been replaced with a combined header, Magister J3.

8. **Four LEDs have been removed**

   Ozy LEDs D5, D6, D7 and D8 have been removed. These were driven by FX2 port pins PE0, PE1, PE2 and PE3, respectively. These FX2 pins still connect to the same FPGA pins as they did on Ozy, but no longer drive LEDs on Magister.

9. **GPIO and DB25 connectors have been removed, and DB9 pins are fixed-configured**

   Ozy GPIO connector J17 and associated pull-down resistors have been removed. Ozy DB25 connector J20 has been removed, along with its associated drivers, R/C filters and pull-up resistors. Ozy FPGA pins FPGA_GPIO1 through FPGA_GPIO12 and FPGA_GPIO17 through FPGA_GPIO21 are now left unconnected on Magister.

   Ozy FPGA pins FPGA_GPIO13 through FPGA_GPIO17 and FPGA_GPIO22 through FPGA_GPIO24 are connected to the same pins on the Magister DB9 connector as they were on Ozy. However, the Magister DB9 outputs on pins 1 - 4 are no longer configurable as either open-collector or totem-pole. Pins 1 and 2 are always open-collector outputs and pins 3 and 4 are always totem-pole outputs. The inputs remain the same, as LVTTL pulled up to 3.3V.

This comparison is between Ozymandias Rev B, 06 Oct 2006 and Magister Rev XA7, 26 Aug 2009. Please refer to the board schematics for further detail.