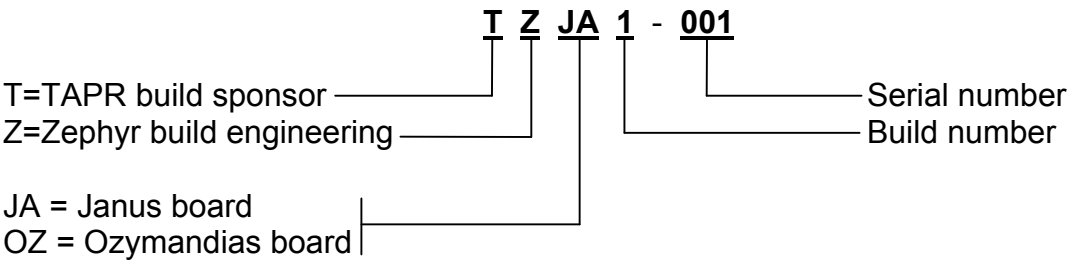
1 Serialization

Boards will be serialized per the following:



2 Test Fixture Descriptions

Each board is tested twice: a bus loop-back test in Test Fixture 1 and a remote loop-back in Test Fixture 2. Power was supplied for all test fixtures by PicoPSU-60-WI 60W supplies running on 12VDC input. You can get them at http://www.mini-box.com

2.1 Test Fixture 1 for Janus and Ozy

Test fixture 1 consists of an ATLAS backplane with a loop-back cable installed. An Ozy serial cable is required for testing Ozy boards, and a Janus PTT cable is required to test Janus boards. Schematics for these are available in the directory “Test_Fixture_Hardware”.

WARNING: To avoid bus contention, plug in only ONE board (Ozy or Janus) when running loop-back tests in Test Fixture 1.

A PC is used to monitor Ozy serial output as well as to program the Ozy serial FPGA load PROM and the Janus CPLD. The PC must have a serial terminal program (such as Hyperterminal) and a fully licensed copy of Quartus II webpack (available free from http://www.altera.com). A ByteBlaster is also required to program the PROM and CPLD.

NOTE: If you do not have a ByteBlaster, you can still run the Ozy bus loop-back test that comes pre-loaded in the PROM. You will not be able to load the loop-back test into the Janus CPLD, so you will not be able to run the Janus bus loop-back test.

2.2 Test Fixture 2 for Janus and Ozy

Test Fixture 2 consists of an ATLAS backplane with a reference oscillator installed in slot 6. A schematic for the reference oscillator plug-in is available in the directory “Test_Fixture_Hardware”. You must have both and Ozy and a Janus plugged into the backplane to run the external loop-back tests. If you are testing an Ozy, you must have a known-good Janus plugged in, and vice-versa.

The Janus board must have two 3.5mm (1/8”) stereo plug to 3.5mm stereo plug jumpers installed:

- J1 (unbal audio) to J5 (line out)
- J4 (mic) to J7 (pwm)

The Janus board must be jumpered this way:

- IC2 BYP: both on (horizontal)

- JP1, JP3, JP4, JP6: on
- JP2, JP5, JP12, MIC BIAS: off
- MIC PTT: 1-2
- MIC AUDIO: 3-4

The Ozy board must be jumpered this way (note that this is different from Test Station 1):

- J32: 1-2
- J23: 3-4
- J24: 1-2

3 Test Fixture Hardware

3.1 Janus Test Fixture Cable

The Janus test fixture cable is just a DB-25F socket that is wired onto the Ozy test fixture cable to test the additional pins that normally go to the Ozy DB-25 connector. Since Janus does not have this connector, we loop J20 pins to other J20 pins or to the DIN+ connector.

Loop-back Cable		Janus PCB Pin/Signal Name		Janus CPLD Pins	
From	To	From	To	From	To
J20F-1	J20F-7	P1-C31/C31	P1-A31/A31	26	27
J20F-3	PLUS_A20	P1-A20/I2CSCK	P1-C20/C20	39	40
J20F-4	PLUS_A21	P1-A21/I2CSDA	P1-C21/C21	37	38
J20F-5	J20F-8	P1-A27/CTDO	P1-C27/C27	25	29
J20F-6	J20F-9	P1-A29/CTDI	P1-C29/C29	23	28

3.2 Janus Reference Oscillator (Test Station 2 Connector)

The Janus reference oscillator for test station 2 is a DIN connector wired with a clock oscillator. The pin connections are shown in the following table. Remember, if you use the same connector as you did for the loop-back cable the pin numbering is backwards from the Atlas bus pin numbers (A1 is A32, A2 is A31, etc). The oscillator should be a 10MHz, 3.3V unit, Epson SG-636PCE 10.0000MC1 (Digi-Key SE2818CT-ND) or equivalent.

You can mount the oscillator right on the connector between the output (C16) and ground (B14) pins and run a wire over to the 3.3V (A30) pin.

OSC pin	Janus DIN Pin	Signal
3	C16	10MHz
2	B14	GND
4	A30	+3.3V

3.3 Ozy Test Fixture Cable

Notes: J8M is a DB-9 male that plugs into Ozy J8; J20M is a DB-25 male that plugs into Ozy J20; pu is 1K to +3.3V on PLUS-A30/C30. See schematic diagram.

You can use Amp P/N 5650908-5 (Mouser P/N 571-565-0908-5) for the PLUS and MINUS DIN connectors, but be aware that the pins on this connector are numbered ***BACKWARDS***. Numbers in the following table correspond to Janus/Ozy/Atlas numbering.

The MINUS DIN connector is typically plugged into ATLAS J1, the board under test into J2 and the PLUS DIN connector into J3. Any three slots are OK, but they must be adjacent with MINUS in a lower-numbered slot and PLUS in a higher-numbered slot.

Loop-back Cable		Ozy PCB Pin/Signal Name		Ozy First Connection		Test Output
From	To	From	To	From	To	
J8M-1 (pu)	J20M-15	J8-1/BGPIO13	J20-15/FPGA_GPIO21	U11-16	R12-5/7	F 22
J8M-2 (pu)	J8M-6	J8-2/BGPIO14	J8-6/FPGA_GPIO22	U11-15	R12-4/8	F 23
J8M-3 (pu)	J8M-7	J8-3/BGPIO15	J8-7/FPGA_GPIO23	U11-14	R12-3/9	F 24
J8M-4 (pu)	J8M-8	J8-4/BGPIO16	J8-8/FPGA_GPIO24	U11-13	R12-2/10	F 25
J20M-1	MINUS-A31	J20-1/FPGA_GPIO9	J31-C31/ATLAS_C31	R10-5/7	U12-103	F 1e
J20M-2	J20M-10	J20-2/FPGA_GPIO1	J20-10/FPGA_GPIO17	R26-5/7	R13-5/7	F 16
J20M-3	PLUS-C20	J20-3/FPGA_GPIO2	J31-C20/ATLAS_C20	R26-4/8	U12-180	F 17
J20M-4	PLUS-C21	J20-4/FPGA_GPIO3	J31-C21/ATLAS_C21	R26-3/9	U12-181	F 18
J20M-5	PLUS-A29	J20-5/FPGA_GPIO4	J31-A27/ATLAS_A27	R26-2/10	U12-104	F 19
J20M-6	MINUS-A27	J20-6/FPGA_GPIO5	J31-A29/ATLAS_A29	R25-5/7	U12-105	F 1a
J20M-7	PLUS-C31	J20-7/FPGA_GPIO6	J31-A31/ATLAS_A31	R25-4/8	U12-192	F 1b
J20M-8	PLUS-C29	J20-8/FPGA_GPIO7	J31-C27/ATLAS_C27	R25-3/9	U12-191	F 1c
J20M-9	MINUS-C27	J20-9/FPGA_GPIO8	J31-C29/ATLAS_C29	R25-2/10	U12-189	F 1d
J20M-11	J20M-14	J20-11/FPGA_GPIO18	J20-14/FPGA_GPIO10	R13-4/8	R10-4/8	F 1f
J20M-12	J20M-16	J20-12/FPGA_GPIO19	J20-16/FPGA_GPIO11	R13-3/9	R10-3/9	F 20
J20M-13	J20M-17	J20-13/FPGA_GPIO20	J20-17/FPGA_GPIO12	R13-2/10	R10-2/10	F 21
PLUS-A30	PLUS-C30	+3.3V	+3.3V	--	--	--
PLUS-A25	PLUS-C25	J31-A25/ATLAS_A25	J31-C25/ATLAS_C25	U12-106	U12-188	F 00
PLUS-A24	PLUS-C24	J31-A24/ATLAS_A24	J31-C24/ATLAS_C24	U12-110	U12-187	F 01
PLUS-A23	PLUS-C23	J31-A23/ATLAS_A23	J31-C23/ATLAS_C23	U12-112	U12-185	F 02
PLUS-A22	PLUS-C22	J31-A22/ATLAS_A22	J31-C22/ATLAS_C22	U12-113	U12-182	F 03
PLUS-A19	PLUS-C19	J31-A19/ATLAS_A19	J31-C19/ATLAS_C19	U12-116	U12-179	F 04
PLUS-A18	PLUS-C18	J31-A18/ATLAS_A18	J31-C18/ATLAS_C18	U12-117	U12-176	F 05
PLUS-A17	PLUS-C17	J31-A17/ATLAS_A17	J31-C17/ATLAS_C17	U12-118	U12-175	F 06
PLUS-A16	PLUS-C16	J31-A16/ATLAS_A16	J31-C16/ATLAS_C16	U12-127	U12-173	F 07
PLUS-A15	PLUS-C15	J31-A15/ATLAS_A15	J31-C15/ATLAS_C15	U12-128	U12-171	F 08
PLUS-A14	PLUS-C14	J31-A14/ATLAS_A14	J31-C14/ATLAS_C14	U12-133	U12-170	F 09
PLUS-A13	PLUS-C13	J31-A13/ATLAS_A13	J31-C13/ATLAS_C13	U12-134	U12-169	F 0a
PLUS-A12	PLUS-C12	J31-A12/ATLAS_A12	J31-C12/ATLAS_C12	U12-135	U12-168	F 0b
PLUS-A11	PLUS-C11	J31-A11/ATLAS_A11	J31-C11/ATLAS_C11	U12-137	U12-165	F 0c
PLUS-A10	PLUS-C10	J31-A10/ATLAS_A10	J31-C10/ATLAS_C10	U12-138	U12-164	F 0d
PLUS-A9	PLUS-C9	J31-A9/ATLAS_A9	J31-C9/ATLAS_C9	U12-139	U12-163	F 0e
PLUS-A8	PLUS-C8	J31-A8/ATLAS_A8	J31-C8/ATLAS_C8	U12-141	U12-162	F 0f
PLUS-A7	PLUS-C7	J31-A7/ATLAS_A7	J31-C7/ATLAS_C7	U12-142	U12-161	F 10
PLUS-A6	PLUS-C6	J31-A6/ATLAS_A6	J31-C6/ATLAS_C6	U12-143	U12-160	F 11
PLUS-A5	PLUS-C5	J31-A5/ATLAS_A5	J31-C5/ATLAS_C5	U12-144	U12-152	F 12
PLUS-A4	PLUS-C4	J31-A4/ATLAS_A4	J31-C4/ATLAS_C4	U12-145	U12-151	F 13
PLUS-A3	PLUS-C3	J31-A3/ATLAS_A3	J31-C3/ATLAS_C3	U12-146	U12-150	F 14
PLUS-A2	PLUS-C2	J31-A2/ATLAS_A2	J31-C2/ATLAS_C2	U12-147	U12-149	F 15

4 Ozy Testing

4.1 Ozy Test Summary

Test #1 covers (*)
Test #2 covers (**)

1. *Power LED (1 red, no test required)
2. *FPGA Debug LEDS (4 red)
3. **FX2 Debug LEDs (6 red)
4. **FPGA Load LED (1 red)
5. *Power-on reset (U9) no test required
6. **USB Port
7. (no test) U2 DS2480B 1-wire driver (Atlas A[18])
8. ** (future) FX2 Serial port RXD0/TXD0 (loop-back at J6?)
9. *FPGA Serial Port RXD2/TXD2 (PC terminal)
10. **U4 24LC128 128Kbit serial EEPROM read/write test
11. (no test) U3 LVDS
12. *U1 FPGA serial EPROM
    a. program through HDR1
    b. load FPGA using active serial mode
13. **Load FPGA through JTAG header HDR2
14. *PIO test: J20 (DB25 loop-back)
15. *PIO test: J8 (DB9 loop-back)
16. (no test) PIO test: J17
17. *Atlas Bus interface
    a. A[2:25], A27], A[29], A[31]
    b. C[2:25], C[27], C[29], C[31]

4.2 Ozy Test Procedure

4.2.1 Visual Inspection and serialization

- Affix S/N barcode label
- Check for solder shorts/opens, especially opens at resistor packs R9, R10, R12, R13, R25, R26.
- Verify jumpers J23 and J24 short pins 2-3 (active serial) and J32 shorts pins 1-2 (bus power)

4.2.2 Test Station 1 Procedure

- Plug board into Atlas only fixture with loop-backs, connect loop-back cable to J8/J20, serial cable to J6 and USB blaster to HDR1
- Power up
- Verify D12 lights (**Power LED**)
- Program Wraptest.pof test code into U1 (**PROM program**)
- Verify LEDs **D1-D4 flash in rotation**
- Verify "**ALL PASS!**" appears on serial port
- Power down and remove board
- Set jumper J24 to short pins 1-2 (Passive Serial)

4.2.3 Test Station 2 Procedure

- Plug board into Atlas/Janus test fixture, USB cable to test PC
- Power up unit
- In the command window, type "**ld1**" to load OZYV1FW.hex firmware into the FX2
- Verify that D9 flashes once per second and look for "Result: True" on console
- Wait for USB to re-enumerate
- In the command window, type "**pg1**" to program the VID/PID into the Ozy EEPROM
- Look for "**Programming Successful!**" on console
- In the command window, type "**ld2**" to Load the ozyfw-sdr1k.hex firmware into the FX2
- Wait for USB to re-enumerate
- Watch for a flash on D11and type "**pg2**" in the command window to load the FPGA test program
- Look for "FPGA LOAD SUCCEEDED!" on console
- Observe D5-D8 solid on while D9 and D10 alternately flash once per second
- In the command window, type "**init**" to run the Ozy initialization program
- Look for "**Wrote to address: 26**" in the last 3 lines on console
- In the command window, type "**jt**" to run the test program
- Hit return to continue
- Wait 10 seconds, then type "**ctrl-c**"
- Observe that the last two frequencies reported by **jt** are the same within 10 Hz

4.2.4 Package PCB for Shipment

- Place board in antistatic bag
- Seal bag with yellow sticker

5 Janus Testing

5.1 Janus Test Summary

Use JTAG to program CPLD, supply 10MHz clock on Atlas bus pin C16.

Test #1 covers (*)
Test #2 covers (**)

1. *Power LEDs (4 red, no test required)
2. *Software controlled LEDs (1 yellow, 1 green)
3. **VCXO, phase lock to Atlas bus clock
4. U13, 1Kbit EEPROM: read/write test (not tested)
5. **PWM output (2 channels)
6. **U8 TLV320 Codec (DC offset and AC tests)
    a. Line In (2 channels) (not tested)
    b. Line out (2 channels)
    c. Mic In (2 channels)
    d. Phones out (2 channels) (not tested)
7. *PTT input
8. **U7, AK5394A A/D (DC offset and AC tests)
    a. Balanced input (from J2) (not tested)
    b. Unbalanced input (from J1)
9. *Atlas Bus interface
    a. P1A
        i. A[2:19]
        ii. A[20], A[21] (I2CSCK, I2CSDA)
        iii. A[22]
        iv. A[23], A[24], A[27], A[29] (CTMS, CTCK, CTDO, CTDI) (not tested)
        v. A[25] (SDOBACK) (not tested)
        vi. A31
    b. P1C
        i. C[2:22], C[31]
        ii. C[23], C[24], C[25], C[27], C[29] (not tested)

5.2 Janus Test Procedure

5.2.1 Visual Inspection and serialization

- Affix S/N barcode label
- Check for solder shorts and opens
- Verify jumpers are set as follows:
    - JP12: off (hang off of pin 2)
    - I2C BYP: both horizontal
    - JP1, JP3, JP4, JP6: on
    - JP2, JP5: off (hang off of pin 1)
    - MIC BIAS: off (hang off of pin 1)
    - MIC PTT: 1-2
    - MIC AUDIO: 2-3

5.2.2 Test Station 1 Procedure

- Plug board into Atlas only fixture with loop-backs, connect loop-back cable to P20 to J20 and USB blaster to P2
- Plug PTT test cable into J4 (MIC)
- Power up and program Janus_wrap.pof test code into U11
- Verify that LED4 and LED5 are alternating
- Press PTT switch and verify that LED4 and LED5 stay on while PTT is pressed
- Program Janus.pof operating code into U11

5.2.3 Test Station 2 Procedure

- Plug board into Atlas/Ozy test fixture, USB cable from Ozy to test PC
- Plug 1/8” loop-back cable between J7 (PWM) and J4 (MIC)
- Plug 1/8” loop-back cable between J5 (LINE OUT) and J1 (UNBAL AUD)
- Power up unit
- Verify LED4 and LED5 both light.
- Open up a command window and type “**ld2**” to load ozyfw-sdr1k.hex into the FX2
- Wait for USB to re-enumerate
- Type “**pg2**” in the command window to load the Ozy FPGA
- Look for “FPGA LOAD SUCCEEDED!” on console
- In the command window, type “**init**” to run the Ozy initialization program
- Look for “**Wrote to address: 26**” in the last 3 lines on console
- In the command window, type “**jt**” to run the test program
- Observe that the frequencies and levels match (both left and right). Levels should be between 0.16 and 0.03, with higher ranges early in the test and lower ranges later. (The test takes about 30 seconds to run.)

5.2.4 Package PCB for Shipment

- Place board in antistatic bag
- Seal bag with yellow sticker