1 Serialization
Boards will be serialized per the following:

T=TAPR build sponsor
Z=Zephyr build engineering
JA = Janus board
OZ = Ozymandias board

T Z JA 1 - 001
Serial number Build number

2 Test Fixture Descriptions
Each board is tested twice: a bus loop-back test in Test Fixture 1 and a remote loop-back in Test Fixture 2. Power was supplied for all test fixtures by PicoPSU-60-WI 60W supplies running on 12VDC input. You can get them at http://www.mini-box.com

2.1 Test Fixture 1 for Janus and Ozy
Test fixture 1 consists of an ATLAS backplane with a loop-back cable installed. An Ozy serial cable is required for testing Ozy boards, and a Janus PTT cable is required to test Janus boards. Schematics for these are available in the directory “Test_Fixture_Hardware”.

WARNING: To avoid bus contention, plug in only ONE board (Ozy or Janus) when running loop-back tests in Test Fixture 1.

A PC is used to monitor Ozy serial output as well as to program the Ozy serial FPGA load PROM and the Janus CPLD. The PC must have a serial terminal program (such as Hyperterminal) and a fully licensed copy of Quartus II webpack (available free from http://www.altera.com). A ByteBlaster is also required to program the PROM and CPLD.

NOTE: If you do not have a ByteBlaster, you can still run the Ozy bus loop-back test that comes pre-loaded in the PROM. You will not be able to load the loop-back test into the Janus CPLD, so you will not be able to run the Janus bus loop-back test.

2.2 Test Fixture 2 for Janus and Ozy
Test Fixture 2 consists of an ATLAS backplane with a reference oscillator installed in slot 6. A schematic for the reference oscillator plug-in is available in the directory “Test_Fixture_Hardware”. You must have both and Ozy and a Janus plugged into the backplane to run the external loop-back tests. If you are testing an Ozy, you must have a known-good Janus plugged in, and vice-versa.

The Janus board must have two 3.5mm (1/8”) stereo plug to 3.5mm stereo plug jumpers installed:
• J1 (unbal audio) to J5 (line out)
• J4 (mic) to J7 (pwm)

The Janus board must be jumpered this way:
• IC2 BYP: both on (horizontal)
• JP1, JP3, JP4, JP6: on
• JP2, JP5, JP12, MIC BIAS: off
• MIC PTT: 1-2
• MIC AUDIO: 3-4

The Ozy board must be jumpered this way (note that this is different from Test Station 1):
• J32: 1-2
• J23: 3-4
• J24: 1-2

3 Test Fixture Hardware

3.1 Janus Test Fixture Cable
The Janus test fixture cable is just a DB-25F socket that is wired onto the Ozy test fixture cable to test the additional pins that normally go to the Ozy DB-25 connector. Since Janus does not have this connector, we loop J20 pins to other J20 pins or to the DIN+ connector.

<table>
<thead>
<tr>
<th>Loop-back Cable</th>
<th>Janus PCB Pin/Signal Name</th>
<th>Janus CPLD Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>From</td>
<td>To</td>
<td>From</td>
</tr>
<tr>
<td>J20F-1</td>
<td>J20F-7</td>
<td>P1-C31/C31</td>
</tr>
<tr>
<td>J20F-3</td>
<td>PLUS_A20</td>
<td>P1-A20/I2CSCK</td>
</tr>
<tr>
<td>J20F-4</td>
<td>PLUS_A21</td>
<td>P1-A21/I2CSDA</td>
</tr>
<tr>
<td>J20F-5</td>
<td>J20F-8</td>
<td>P1-A27/CTDO</td>
</tr>
<tr>
<td>J20F-6</td>
<td>J20F-9</td>
<td>P1-A29/CTDI</td>
</tr>
</tbody>
</table>

3.2 Janus Reference Oscillator (Test Station 2 Connector)
The Janus reference oscillator for test station 2 is a DIN connector wired with a clock oscillator. The pin connections are shown in the following table. Remember, if you use the same connector as you did for the loop-back cable the pin numbering is backwards from the Atlas bus pin numbers (A1 is A32, A2 is A31, etc). The oscillator should be a 10MHz, 3.3V unit, Epson SG-636PCE 10.0000MC1 (Digi-Key SE2818CT-ND) or equivalent.

You can mount the oscillator right on the connector between the output (C16) and ground (B14) pins and run a wire over to the 3.3V (A30) pin.

<table>
<thead>
<tr>
<th>OSC pin</th>
<th>Janus DIN Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>C16</td>
<td>10MHz</td>
</tr>
<tr>
<td>2</td>
<td>B14</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>A30</td>
<td>+3.3V</td>
</tr>
</tbody>
</table>
3.3 Ozy Test Fixture Cable

Notes: J8M is a DB-9 male that plugs into Ozy J8; J20M is a DB-25 male that plugs into Ozy J20; pu is 1K to +3.3V on PLUS-A30/C30. See schematic diagram.

You can use Amp P/N 5650908-5 (Mouser P/N 571-565-0908-5) for the PLUS and MINUS DIN connectors, but be aware that the pins on this connector are numbered **BACKWARDS**. Numbers in the following table correspond to Janus/Ozy/Atlas numbering.

The MINUS DIN connector is typically plugged into ATLAS J1, the board under test into J2 and the PLUS DIN connector into J3. Any three slots are OK, but they must be adjacent with MINUS in a lower-numbered slot and PLUS in a higher-numbered slot.

<table>
<thead>
<tr>
<th>Loop-back Cable</th>
<th>Ozy PCB Pin/Signal Name</th>
<th>Ozy First Connection</th>
<th>Test Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>From</td>
<td>To</td>
<td>From</td>
<td>To</td>
</tr>
<tr>
<td>J20M-1</td>
<td>MINUS-A31</td>
<td>J20-1/FPGA_GPIO9</td>
<td>J31-31/ATLAS_C31</td>
</tr>
<tr>
<td>J20M-2</td>
<td>J20M-10</td>
<td>J20-10/FPGA_GPIO17</td>
<td>R26-5/7 U13-5/7 F 16</td>
</tr>
<tr>
<td>J20M-6</td>
<td>MINUS-A27</td>
<td>J20-6/FPGA_GPIO5</td>
<td>J31-A29/ATLAS_A29</td>
</tr>
<tr>
<td>J20M-7</td>
<td>PLUS-C31</td>
<td>J20-7/FPGA_GPIO6</td>
<td>J31-A31/ATLAS_A31</td>
</tr>
<tr>
<td>J20M-8</td>
<td>PLUS-C29</td>
<td>J20-8/FPGA_GPIO7</td>
<td>J31-C27/ATLAS_C27</td>
</tr>
<tr>
<td>J20M-9</td>
<td>MINUS-C27</td>
<td>J20-9/FPGA_GPIO8</td>
<td>J31-C29/ATLAS_C29</td>
</tr>
<tr>
<td>J20M-11</td>
<td>J20M-14</td>
<td>J20-14/FPGA_GPIO10</td>
<td>R13-4/8 R10-4/8 F 1f</td>
</tr>
<tr>
<td>J20M-13</td>
<td>J20M-17</td>
<td>J20-17/FPGA_GPIO12</td>
<td>R13-2/10 R10-2/10 F 21</td>
</tr>
<tr>
<td>PLUS-A25</td>
<td>PLUS-C30</td>
<td></td>
<td>+3.3V</td>
</tr>
<tr>
<td>PLUS-A22</td>
<td>PLUS-C23</td>
<td>J31-A23/ATLAS_A23</td>
<td>J31-C23/ATLAS_C23</td>
</tr>
<tr>
<td>PLUS-A19</td>
<td>PLUS-C19</td>
<td>J31-A19/ATLAS_A19</td>
<td>J31-C19/ATLAS_C19</td>
</tr>
<tr>
<td>PLUS-A18</td>
<td>PLUS-C18</td>
<td>J31-A18/ATLAS_A18</td>
<td>J31-C18/ATLAS_C18</td>
</tr>
<tr>
<td>PLUS-A17</td>
<td>PLUS-C17</td>
<td>J31-A17/ATLAS_A17</td>
<td>J31-C17/ATLAS_C17</td>
</tr>
<tr>
<td>PLUS-A16</td>
<td>PLUS-C16</td>
<td>J31-A16/ATLAS_A16</td>
<td>J31-C16/ATLAS_C16</td>
</tr>
<tr>
<td>PLUS-A15</td>
<td>PLUS-C15</td>
<td>J31-A15/ATLAS_A15</td>
<td>J31-C15/ATLAS_C15</td>
</tr>
<tr>
<td>PLUS-A14</td>
<td>PLUS-C14</td>
<td>J31-A14/ATLAS_A14</td>
<td>J31-C14/ATLAS_C14</td>
</tr>
<tr>
<td>PLUS-A13</td>
<td>PLUS-C13</td>
<td>J31-A13/ATLAS_A13</td>
<td>J31-C13/ATLAS_C13</td>
</tr>
<tr>
<td>PLUS-A12</td>
<td>PLUS-C12</td>
<td>J31-A12/ATLAS_A12</td>
<td>J31-C12/ATLAS_C12</td>
</tr>
<tr>
<td>PLUS-A11</td>
<td>PLUS-C11</td>
<td>J31-A11/ATLAS_A11</td>
<td>J31-C11/ATLAS_C11</td>
</tr>
<tr>
<td>PLUS-A10</td>
<td>PLUS-C10</td>
<td>J31-A10/ATLAS_A10</td>
<td>J31-C10/ATLAS_C10</td>
</tr>
<tr>
<td>PLUS-A9</td>
<td>PLUS-C9</td>
<td>J31-A9/ATLAS_A9</td>
<td>J31-C9/ATLAS_C9</td>
</tr>
<tr>
<td>PLUS-A8</td>
<td>PLUS-C8</td>
<td>J31-A8/ATLAS_A8</td>
<td>J31-C8/ATLAS_C8</td>
</tr>
<tr>
<td>PLUS-A7</td>
<td>PLUS-C7</td>
<td>J31-A7/ATLAS_A7</td>
<td>J31-C7/ATLAS_C7</td>
</tr>
<tr>
<td>PLUS-A5</td>
<td>PLUS-C5</td>
<td>J31-A5/ATLAS_A5</td>
<td>J31-C5/ATLAS_C5</td>
</tr>
<tr>
<td>PLUS-A2</td>
<td>PLUS-C2</td>
<td>J31-A2/ATLAS_A2</td>
<td>J31-C2/ATLAS_C2</td>
</tr>
</tbody>
</table>
4 Ozy Testing

4.1 Ozy Test Summary

Test #1 covers (*)
Test #2 covers (**) 

1. *Power LED (1 red, no test required)
2. *FPGA Debug LEDS (4 red)
3. **FX2 Debug LEDs (6 red)
4. **FPGA Load LED (1 red)
5. *Power-on reset (U9) no test required
6. **USB Port
8. ** (future) FX2 Serial port RXD0/TXD0 (loop-back at J6?)
9. *FPGA Serial Port RXD2/TXD2 (PC terminal)
10. **U4 24LC128 128Kbit serial EEPROM read/write test
11. (no test) U3 LVDS
12. *U1 FPGA serial EPROM
   a. program through HDR1
   b. load FPGA using active serial mode
13. **Load FPGA through JTAG header HDR2
14. *PIO test: J20 (DB25 loop-back)
15. *PIO test: J8 (DB9 loop-back)
16. (no test) PIO test: J17
17. *Atlas Bus interface
   b. C[2:25], C[27], C[29], C[31]
4.2 Ozy Test Procedure

4.2.1 Visual Inspection and serialization
- Affix S/N barcode label
- Check for solder shorts/opens, especially opens at resistor packs R9, R10, R12, R13, R25, R26.
- Verify jumpers J23 and J24 short pins 2-3 (active serial) and J32 shorts pins 1-2 (bus power)

4.2.2 Test Station 1 Procedure
- Plug board into Atlas only fixture with loop-backs, connect loop-back cable to J8/J20, serial cable to J6 and USB blaster to HDR1
- Power up
- Verify D12 lights (Power LED)
- Program Wraptoptest.pof test code into U1 (PROM program)
- Verify LEDs D1-D4 flash in rotation
- Verify “ALL PASS!” appears on serial port
- Power down and remove board
- Set jumper J24 to short pins 1-2 (Passive Serial)

4.2.3 Test Station 2 Procedure
- Plug board into Atlas/Janus test fixture, USB cable to test PC
- Power up unit
- In the command window, type “ld1” to load OZYV1FW.hex firmware into the FX2
- Verify that D9 flashes once per second and look for “Result: True” on console
- Wait for USB to re-enumerate
- In the command window, type “pg1” to program the VID/PID into the Ozy EEPROM
- Look for “Programming Successful!” on console
- In the command window, type “ld2” to Load the ozyfw-sdr1k.hex firmware into the FX2
- Wait for USB to re-enumerate
- Watch for a flash on D11 and type “pg2” in the command window to load the FPGA test program
- Look for “FPGA LOAD SUCCESSEDE!” on console
- Observe D5-D8 solid on while D9 and D10 alternately flash once per second
- In the command window, type “init” to run the Ozy initialization program
- Look for “Wrote to address: 26” in the last 3 lines on console
- In the command window, type “jt” to run the test program
- Hit return to continue
- Wait 10 seconds, then type “ctrl-c”
- Observe that the last two frequencies reported by jt are the same within 10 Hz

4.2.4 Package PCB for Shipment
- Place board in antistatic bag
- Seal bag with yellow sticker
5 Janus Testing

5.1 Janus Test Summary
Use JTAG to program CPLD, supply 10MHz clock on Atlas bus pin C16.

Test #1 covers (*)
Test #2 covers (**)

1. *Power LEDs (4 red, no test required)
2. *Software controlled LEDs (1 yellow, 1 green)
3. **VCXO, phase lock to Atlas bus clock
4. U13, 1Kbit EEPROM: read/write test (not tested)
5. **PWM output (2 channels)
6. **U8 TLV320 Codec (DC offset and AC tests)
   a. Line In (2 channels) (not tested)
   b. Line out (2 channels)
   c. Mic In (2 channels)
   d. Phones out (2 channels) (not tested)
7. *PTT input
8. **U7, AK5394A A/D (DC offset and AC tests)
   a. Balanced input (from J2) (not tested)
   b. Unbalanced input (from J1)
9. *Atlas Bus interface
   a. P1A
      i. A[2:19]
      iii. A[22]
      vi. A31
   b. P1C
      i. C[2:22], C[31]
      ii. C[23], C[24], C[25], C[27], C[29] (not tested)
5.2 Janus Test Procedure

5.2.1 Visual Inspection and serialization

- Affix S/N barcode label
- Check for solder shorts and opens
- Verify jumpers are set as follows:
  - JP12: off (hang off of pin 2)
  - I2C BYP: both horizontal
  - JP2, JP5: off (hang off of pin 1)
  - MIC BIAS: off (hang off of pin 1)
  - MIC PTT: 1-2
  - MIC AUDIO: 2-3

5.2.2 Test Station 1 Procedure

- Plug board into Atlas only fixture with loop-backs, connect loop-back cable to P20 to J20 and USB blaster to P2
- Plug PTT test cable into J4 (MIC)
- Power up and program Janus_wrap.pof test code into U11
- Verify that LED4 and LED5 are alternating
- Press PTT switch and verify that LED4 and LED5 stay on while PTT is pressed
- Program Janus.pof operating code into U11

5.2.3 Test Station 2 Procedure

- Plug board into Atlas/Ozy test fixture, USB cable from Ozy to test PC
- Plug 1/8" loop-back cable between J7 (PWM) and J4 (MIC)
- Plug 1/8" loop-back cable between J5 (LINE OUT) and J1 (UNBAL AUD)
- Power up unit
- Verify LED4 and LED5 both light.
- Open up a command window and type "ld2" to load ozyfw-sdr1k.hex into the FX2
- Wait for USB to re-enumerate
- Type "pg2" in the command window to load the Ozy FPGA
- Look for "FPGA LOAD SUCCEEDED!" on console
- In the command window, type "init" to run the Ozy initialization program
- Look for "Wrote to address: 26" in the last 3 lines on console
- In the command window, type "jt" to run the test program
- Observe that the frequencies and levels match (both left and right). Levels should be between 0.16 and 0.03, with higher ranges early in the test and lower ranges later. (The test takes about 30 seconds to run.)

5.2.4 Package PCB for Shipment

- Place board in antistatic bag
- Seal bag with yellow sticker