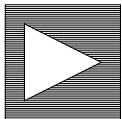


AD6636 CUSTOMER EVALUATION BOARD REV 01B

CONTENTS

- Page 1: AD6636 and its microport header, JTAG header, CHIP\_ID, EXPonent bits, Thermal Diode and Serial Port settings.
- Page 2: CMOS Input Port A, D-Type Flip Flop to buffer before AD6636, LVDS input port (for ports C and D) and CMOS/LVDS clock delay/selection
- Page 3: CMOS Input Port B, D-Type Flip Flop to buffer before AD6636 and FPGA (bypss mode), and CMOS/LVDS clock delay/selection
- Page 4: Altera Apex 20K FPGA. I/O banks 1, 2, 3, and 4 shown, Debug Header for FPGA.
- Page 5: Altera Apex 20K FPGA I/O banks 5, 6, 7 and 8. JTAG and programming headers also shown
- Page 6: FIFO IDT72V273, Parallel Port header for parallel port B, Parallel port clock delays.
- Page 7: Cypress CY7C68013 USB microcontroller. EEPROM for USB enumeration, 24MHz crystal and USB header.
- Page 8: Voltage regulators for 5V, 3.3V, and 1.8V. PC parallel port connector and parallel port transceiver 74LVX161284A



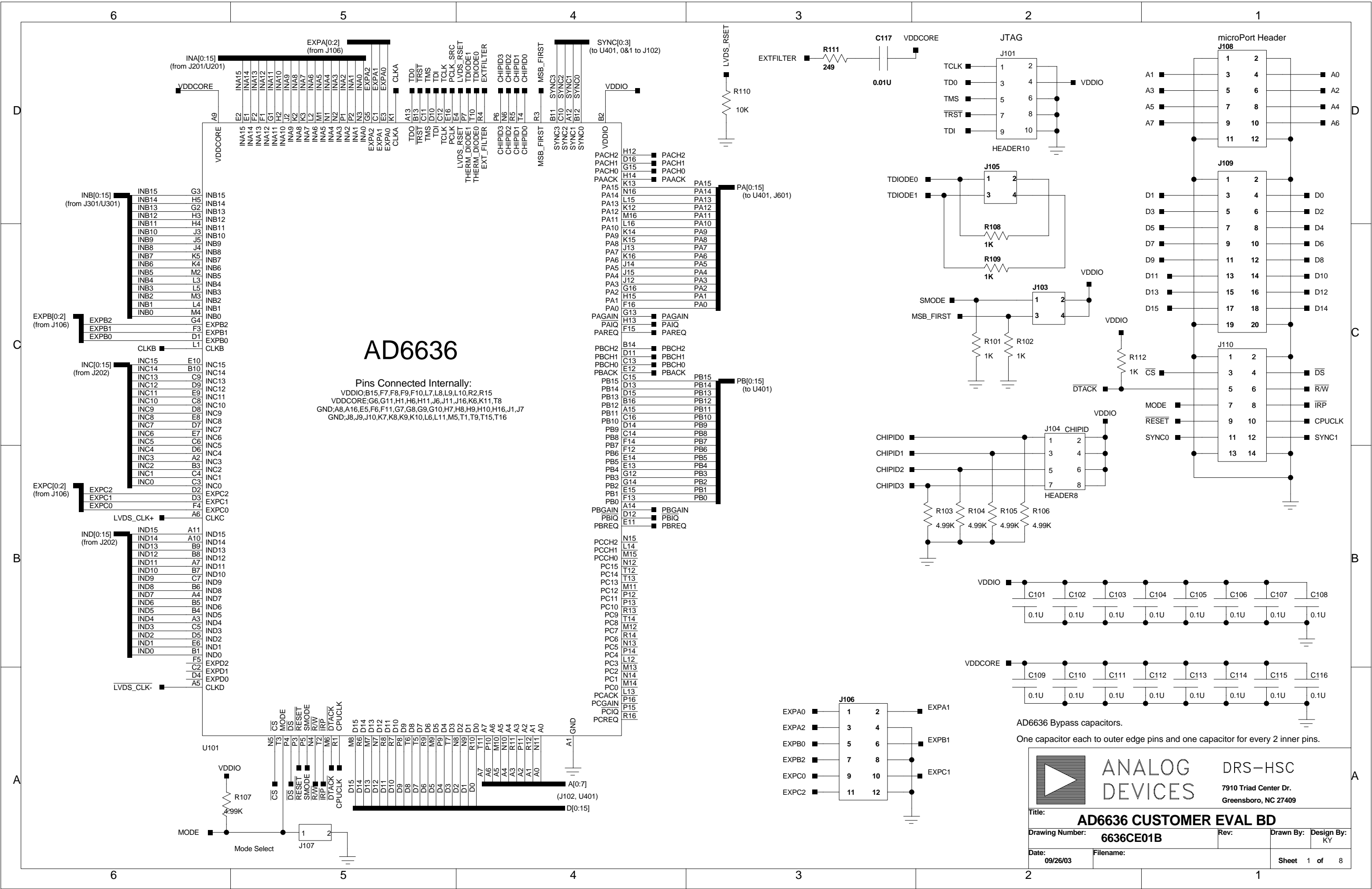
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DRS—HSC  
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Greensboro, NC 27409

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Drawing Number: 6636CE01B	Rev: A	Drawn By: PLL	Design By: KY
Date:	Filename:		Sheet of

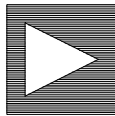
# AD6636

Pins Connected Internally:  
VDDIO:B15,F7,F8,F9,F10,L7,L8,L9,L10,R2,R15  
VDDCORE:G6,G11,H1,H6,H11,J6,J11,J16,K6,K11,T8  
GND:A8,A16,E5,F6,F11,G7,G8,G9,G10,H7,H8,H9,H10,H16,J1,J7  
GND:J8,J9,J10,K7,K8,K9,K10,L6,L11,M5,T1,T9,T15,T16



AD6636 Bypass capacitors.

One capacitor each to outer edge pins and one capacitor for every 2 inner pins.



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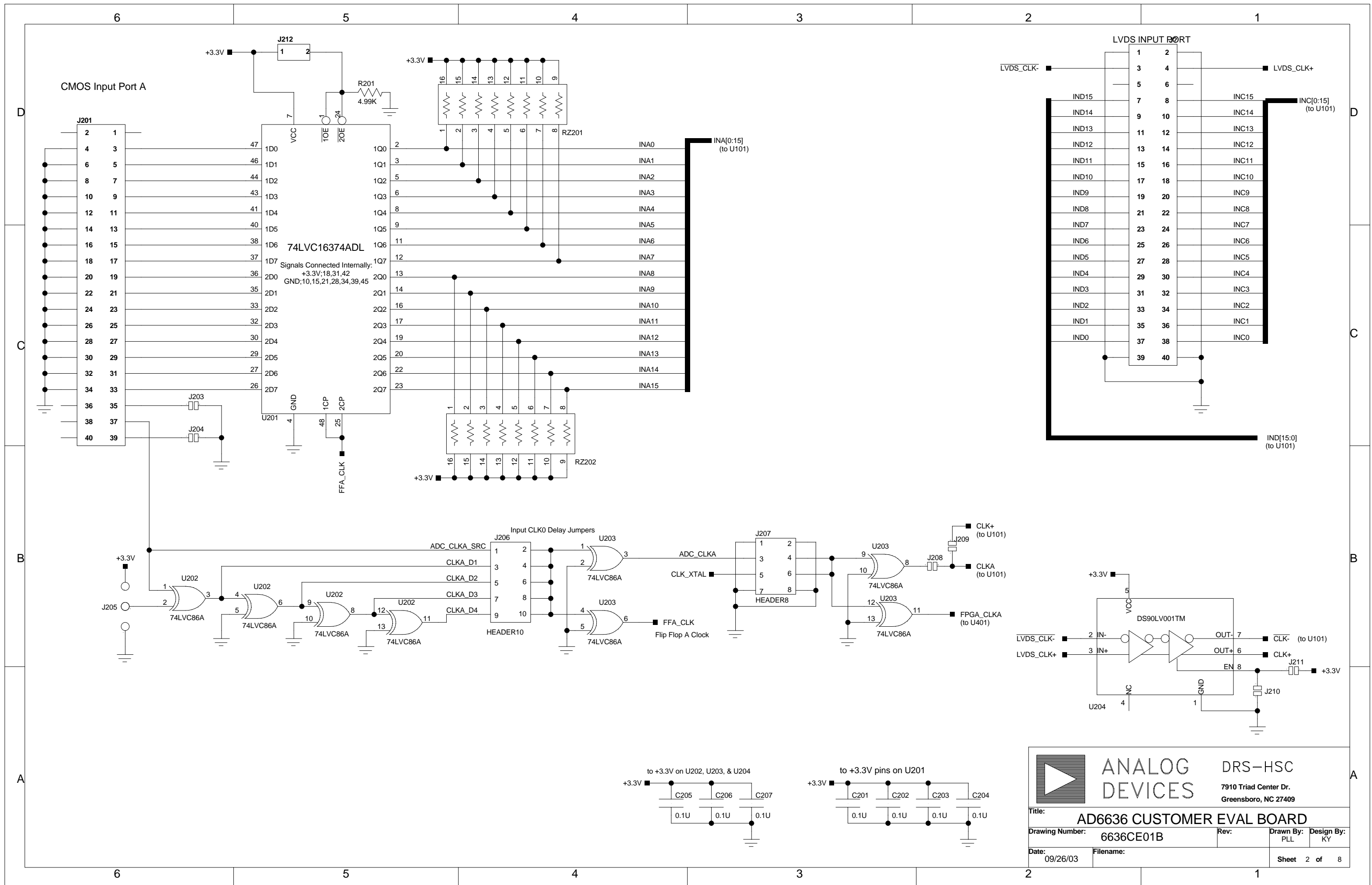
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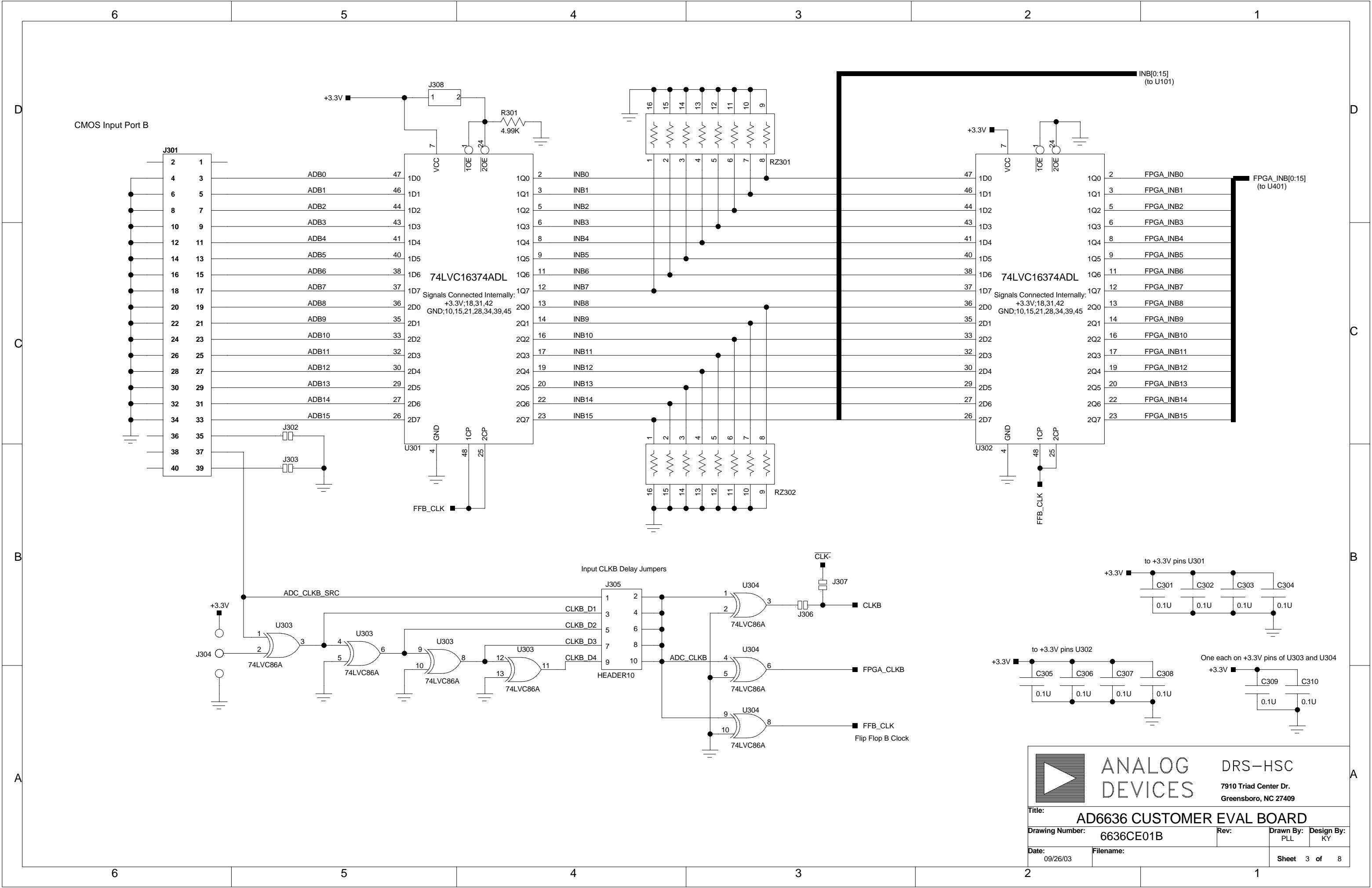
KY

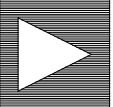
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Sheet 1 of 8







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Rev:

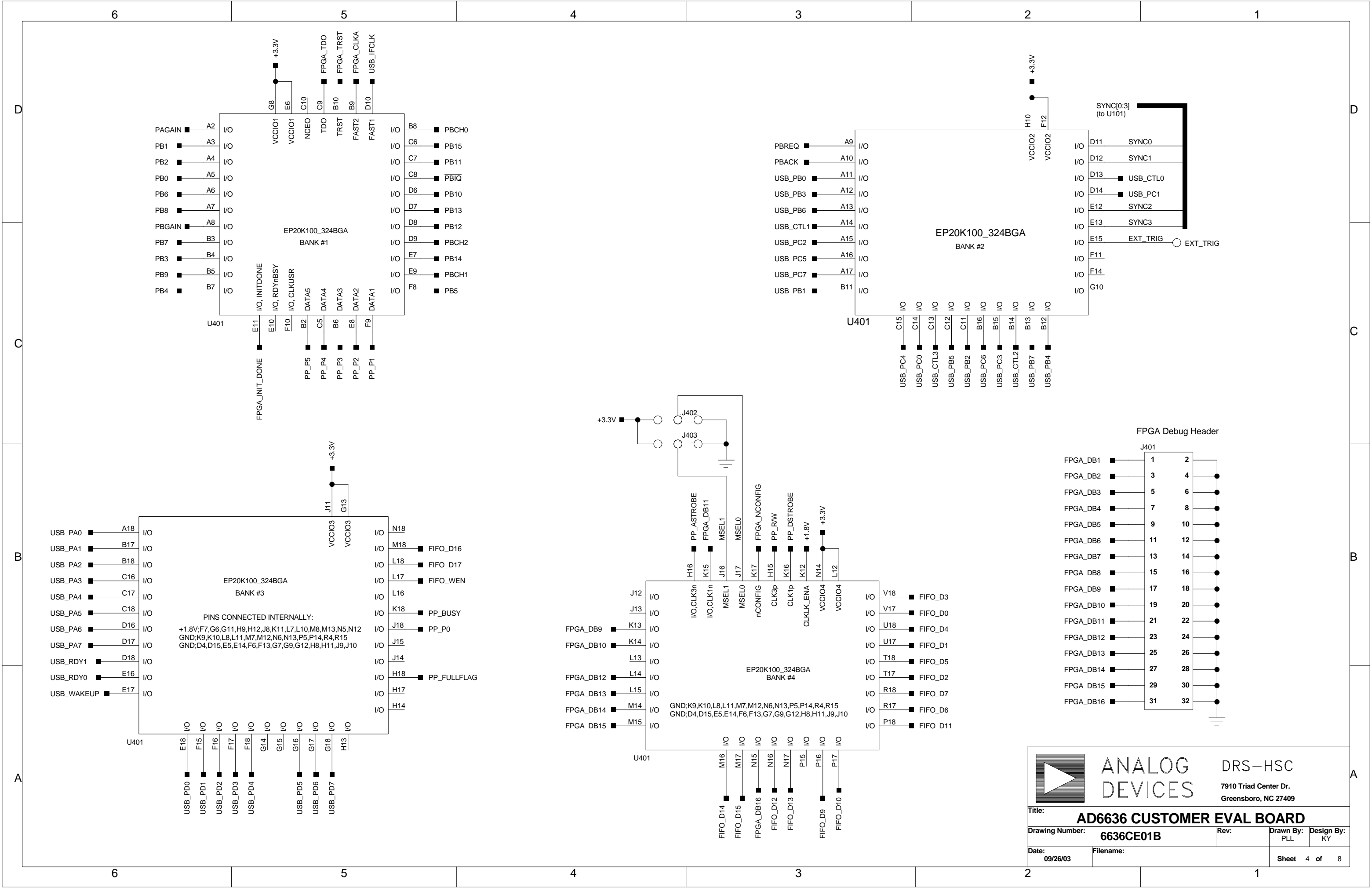
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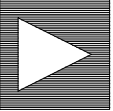
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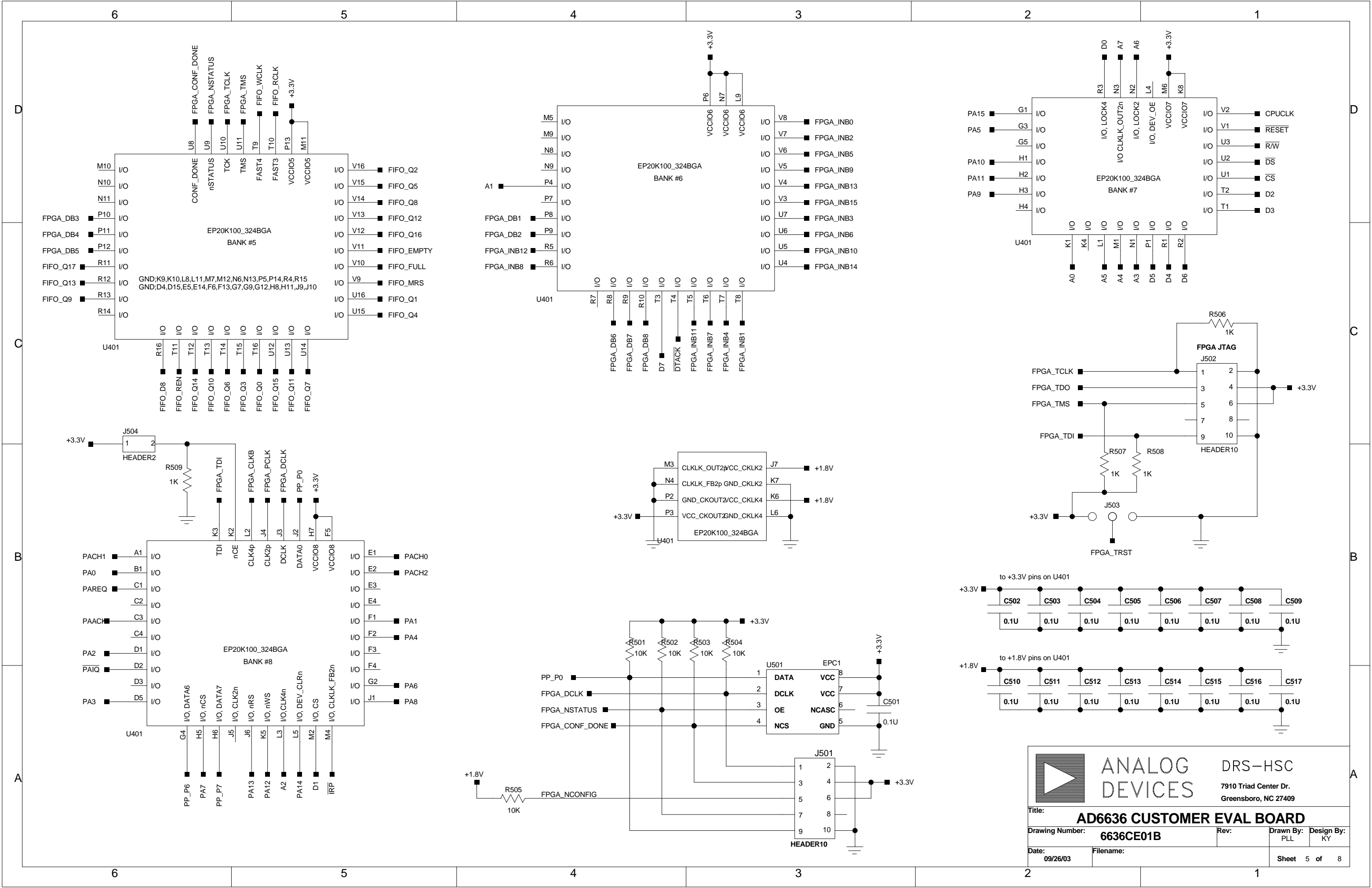
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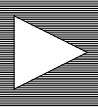
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5 of 8

