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PHILIPS

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1. Introduction

The Peripheral Component Interconnect (PCI) Express Physical (PHY) layer handles the low-level PCI Express protocol and signaling. The main function of the PHY is to convert digital data into electrical signals and vice versa. Intel recommends the PHY Interface for PCI Express Architecture (PIPE) as the digital interface between the PHY and the Media Access Control (MAC) layer. The PXPIPE interface proposed by Philips is a superset of the PIPE specification.

While the PIPE interface uses one clock (PCLK) for both transmit and receive data, PXPIPE introduces source-synchronous clocks for both transmit and receive domains. This makes data and clock synchronization easier and more robust for off-chip data transfer.

PIPE is more conducive to IP-to-IP interface on the same die, while PXPIPE is an elegant enhancement to the PIPE interface to accommodate device-to-device data transfers at very high speed.

This document provides an overview of PXPIPE, and discusses the differences between PXPIPE and PIPE.

2. PXPIPE overview

The PXPIPE interface uses 8-bit input and 8-bit output words, each with control signals and source-synchronous clocks. The data rate is 250 MB/s. PXPIPE operates at the SSTL_2 (Stub Series Terminated Logic for 2.5 Volts) logic level.

Fig 1 shows the PXPIPE interface.

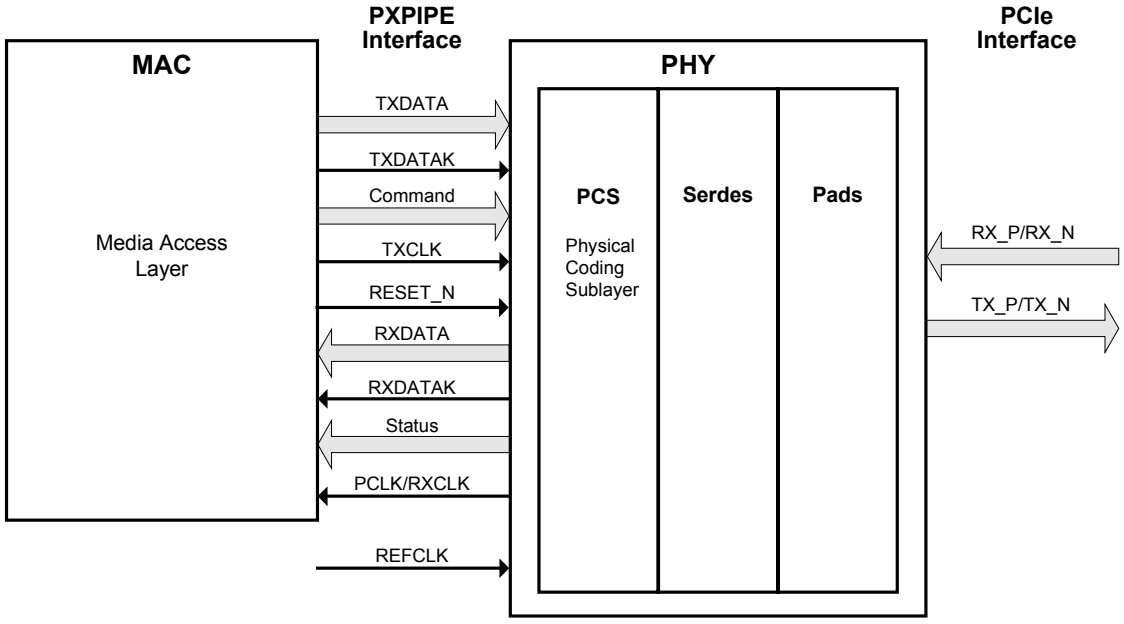

Fig 1. PXPIPE interface

The PHY input and output signals are described in the following tables. Note that direction is defined from the perspective of the PHY. Therefore, a signal described as an “Output” is driven by the PHY and a signal described as an “Input” is received by the PHY. A basic description of each signal is provided.

Table 1: Transmit data interface signals

Name	Direction	Active Level	Description
TXDATA[7:0]	Input	N/A	8-bit transmit data from the MAC to the PHY.
TXDATAK	Input	N/A	Data or control for the symbols of transmit data. A value of 0 indicates a data byte; a value of 1 indicates a control byte.

Table 2: Receive data interface signals

Name	Direction	Active Level	Description
RXDATA[7:0]	Output	N/A	8-bit receive data from the PHY to the MAC.
RXDATAK	Output	N/A	Data or control bit for the symbols of receive data. A value of 0 indicates a data byte; a value of 1 indicates a control byte.

Table 3: Command interface signals

Name	Direction	Active Level	Description
RXDET_LOOPB	Input	HIGH	Instructs the PHY to begin a receiver detection operation or to begin loopback.
TXIDLE	Input	HIGH	Forces TX output to electrical idle when asserted in all power states. When de-asserted while in P0 (as indicated by the PWRDWN signals), indicates that there is valid data present on the TXDATA and TXDATAK pins and that the data should be transmitted. When de-asserted in P2, the signal has no function. It would be used to indicate that the PHY should begin transmitting beacon signaling; however beacon is not supported in this version of the PHY. TXIDLE must always be asserted while in power states P0s and P1.
TXCOMP	Input	HIGH	When HIGH, sets the running disparity to negative. Used when transmitting the compliance pattern.
RXPOL	Input	HIGH	Signals the PHY to perform a polarity inversion on the received data. 0 PHY does no polarity inversion. 1 PHY does polarity inversion.

Name	Direction	Active Level	Description
RESET_N	Input	LOW	Resets the PHY
PWRDWN1, PWRDWN0	Input	N/A	Power up or down the transceiver. Power states: **[1] [0] Description** 0 0 P0, normal operation. 0 1 P0s, low recovery time (2.5 µs) power saving state. 1 0 P1, longer recovery time (64 µs max) lower power state. 1 1 P2, lowest power state.

Table 4: Status interface signals

Name	Direction	Active Level	Description
RXVALID	Output	HIGH	Indicates symbol lock and valid data on RXDATA and RXDATAK.
PHYSTATUS	Output	HIGH	Communicates completion of several PHY functions, including power management state transitions, and receiver detection.
RXIDLE	Output	HIGH	Indicates receiver detection of an electrical idle. This is an asynchronous signal.
RXSTATUS2, RXSTATUS1, RXSTATUS0	Output	N/A	Encodes receiver status and error codes for the received data stream and receiver detection. **[2] [1] [0] Description** 0 0 0 Received data OK 0 0 1 1 SKP added 0 1 0 1 SKP removed 0 1 1 Receiver detected 1 0 0 8 B or 10 B decode error 1 0 0 Elastic Buffer overflow 1 1 0 Elastic Buffer underflow 1 1 1 Receive disparity error

Table 5: Clock signals

Name	Direction	Active Level	Description
REFCLK	Input	Rising Edge	100 MHz reference clock. The PCLK and the bit rate clock are derived from this clock.
TXCLK	Input	Rising Edge	Source-synchronous 250 MHz clock for transmit from the MAC. All data and input signals to the PHY are synchronized to this clock.

Name	Direction	Active Level	Description
PCLK/RXCLK	Output	Rising Edge	Source-synchronous 250 MHz clock for received data bound for the MAC, and can be used by the MAC to clock its internal logic.

3. PXPIPE vs. PIPE

3.1 Data width

PIPE can utilize an 8-bit or 16-bit parallel interface to transmit and receive PCI Express data. PXPIPE can function only as an 8-bit, 250 MB/s interface.

From the application point of view, an 8-bit interface is preferred over 16-bit because of its smaller package and fewer pins, which minimize Printed Circuit Board (PCB) routing overhead. Also, a 16-bit interface inevitably introduces extra latency because of its extra layer of logic. The advantage of a 16-bit interface is its lower frequency.

3.2 Clocking

Two clock signals are used by the PIPE interface component:

- The 100 MHz input reference clock is used by the PHY to generate the internal bit rate clocks for transmitting and receiving data. This clock may have spread spectrum modulation that matches a system reference clock (for example, REFCLK from the Card Electro-Mechanical Specification).
- The parallel interface clock (PCLK), an output of the PHY, is used to synchronize data transfers across the parallel interface. This clock runs at 125 MHz for 16-bit implementations and 250 MHz for 8-bit implementations. The rising edge of the clock is the reference point. This clock may have spread spectrum modulation. When the PHY is reset, PCLK runs at any frequency less than or equal to final operational frequency before it is stable.

Because transmit data is required to be synchronized to the PCLK, the MAC uses PCLK to clock out the TXDATA. The round trip transmission delay between the PHY and the MAC must be less than 1 PCLK period, which is 4 ns for the 250 MHz PCLK.

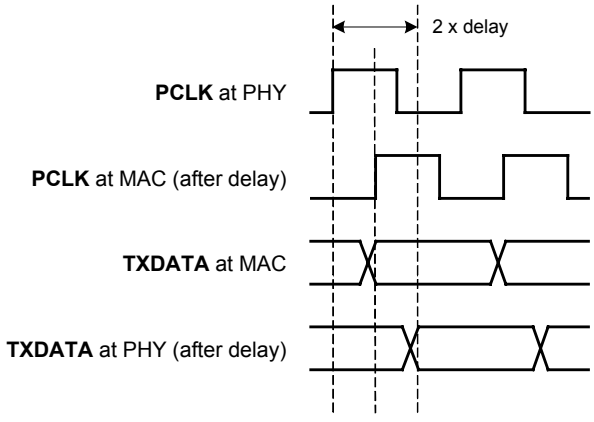

Fig 2. PIPE clocking

Three clock signals are used by PXPIPE:

- The 100 MHz input reference clock, REFCLK, generates the 250 MHz clock and the internal bit rate clock. This clock may have spread spectrum modulation.
- Two source-synchronous clocks for RXDATA and TXDATA are used to simplify timing closure.
  - PCLK/RXCLK, a source-synchronous clock to the MAC, is an output of the PHY. All RXDATA and status signals, except RXIDLE, are synchronous to this clock, which is derived from the internal transmit byte rate clock. The rising edge is centered with respect to the data. When the PHY is reset, it takes the PHY 64 µs maximum to stabilize its internal clocks. PCLK/RXCLK can run from 0 MHz to 275 MHz during this time.
  - TXCLK, a reference clock used by the PHY to clock TXDATA and commands, is an output of the MAC. This source-synchronous clock has the same latency as the data, and the rising edge is centered with respect to the data.

Because both TXDATA and TXCLK are transmitted from the MAC and are source-synchronous, the transmission delay between the PHY and the MAC has the same effect on TXDATA and TXCLK, and will not cause a timing problem. This allows for more robust off-chip communication.

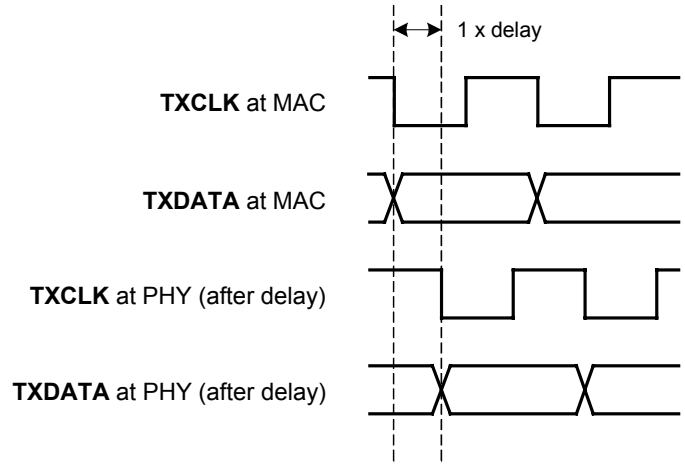

Fig 3. PXPIPE clocking

3.3 Receiver detection

In the PXPIPE interface, when the PHY has completed the receiver detection sequence it asserts PHYSTATUS, and RXSTATUS changes much earlier than PHYSTATUS. The MAC uses the rising edge of PHYSTATUS to sample the RXSTATUS signals, and then it may de-assert RXDET_LOOPB at any time without a max or min time limit. A few cycles after RXDET_LOOPB is de-asserted, PHYSTATUS is de-asserted in response.

In the PIPE specification, the PHY drives RXSTATUS signals to the appropriate code at the same time as it asserts PHYSTATUS for one clock. There is no timing specification for the MAC to sample RXSTATUS signals. PHYSTATUS is simply pulsed for one clock cycle, and there is no handshaking between PHYSTATUS and RXDET_LOOPB.

Fig 4 shows the PXPIPE receiver detection sequence.

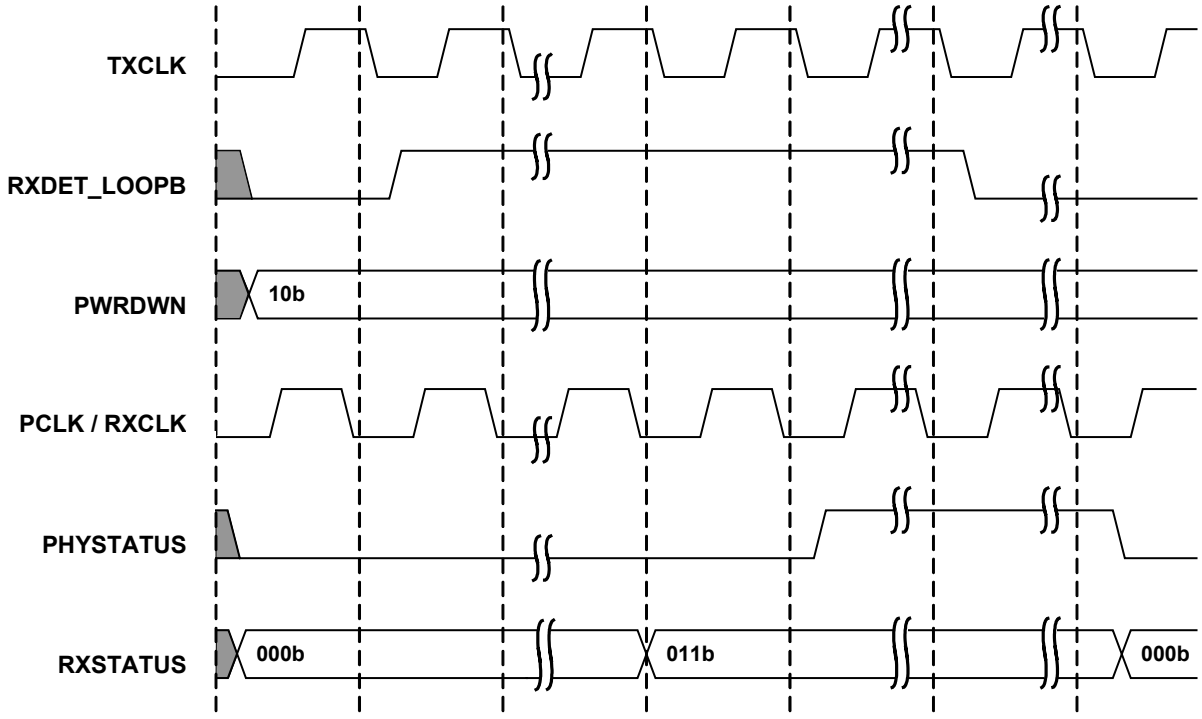

Fig 4. PXPIPE receiver detection sequence

4. Summary

The PXPIPE interface is a superset of the PIPE specification. PXPIPE is enhanced and adapted for a stand-alone PHY, and provides more robust data transfer for off-chip applications.

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7. Contents

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