ASIX Electronics

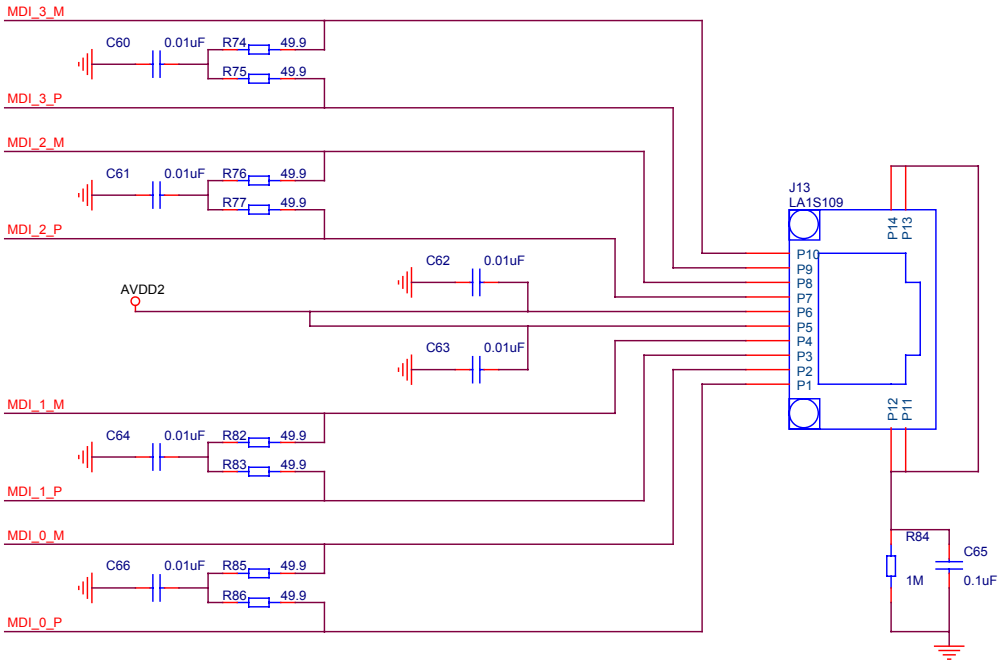
# Layout Guide for AX88180

May ,2006 ,v1.0 Application Note

AX88180 is a high-performance and cost-effective non-PCI Gigabit Ethernet controller for various embedded systems. This document highlights the general layout rules which designer must follow the recommendations in this document.

## Points to remember

Rules need to remember when place the parts on PCB



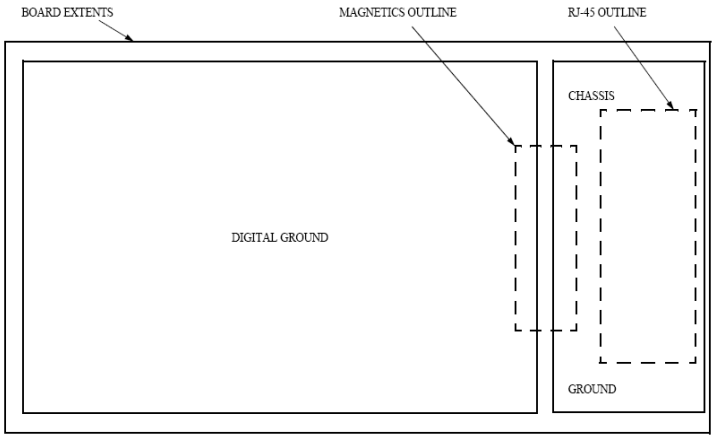

1. Follow above schematic's connection to suppress noise
2. All the parts should place as close as possible. (AX88180 chip, LAN transformer and RJ-45)
3. Oscillator should far away from TX+/-, RX+/- pairs
4. Block A should close to LAN chip (PHY) and block B should close to LAN transformer
5. The trace length from LAN chip to Magnetic should not excess 12 cm, keep the trace as straight as possible, and keep it parallel for differential pairs
6. Keep TX, RX differential signals running symmetric, equal length, and

closely (the trace spacing between the pair should with 2mm, the spacing between 2 pairs should bigger then 5 mm).

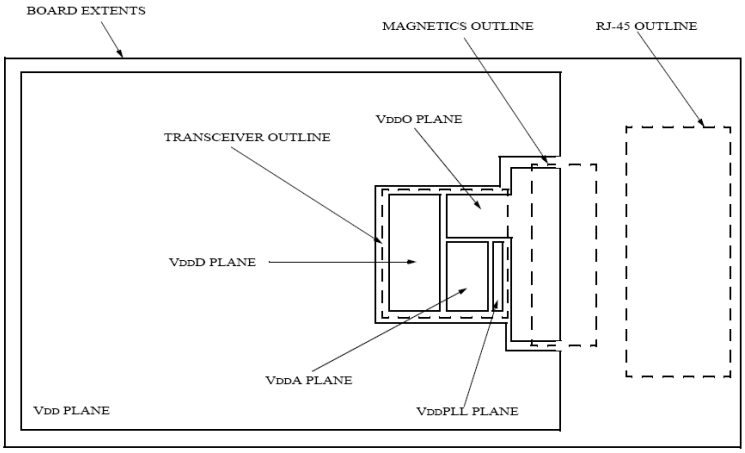
7. Keep RX signal on the top layer, RX signal avoid any VIA
8. Avoid right angle signal trace
9. Avoid signal over power plane.

## Power's consideration

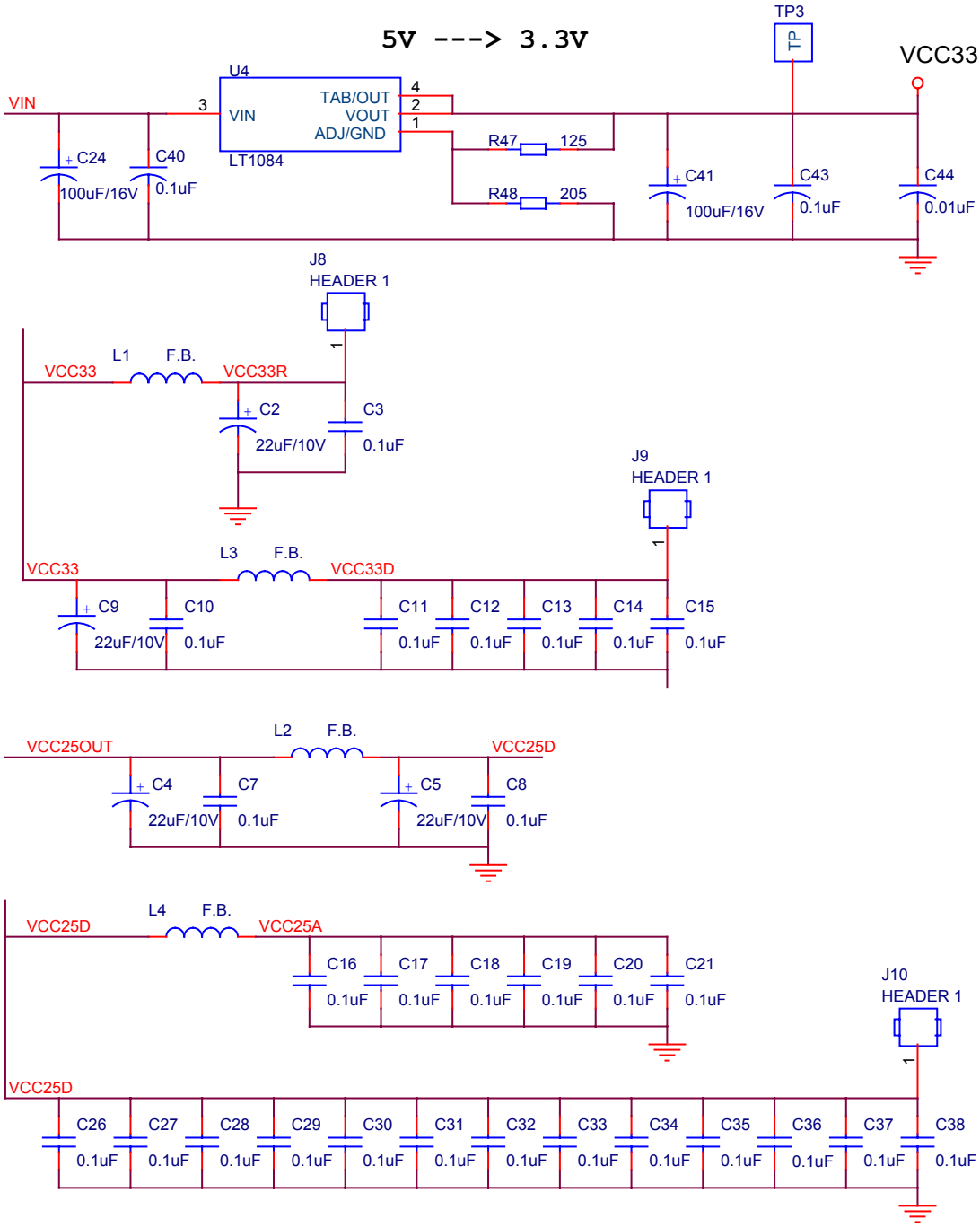
10. Isolate RJ45 connector ground from system ground like following




11. Separate all digital, analog and PLL power/GND plane



## 12. System power connect recommendation



## EMI's consideration

13. The chosen connector must be shielded so that EMI integrity of the design is not compromised. The shield must be electrically connected to chassis ground to extend the chassis barrier for high frequency emissions. If an unshielded connector were used, the EMI would pass through the nylon material of the connector. The shield will also prevent less external EMI from entering the chassis.
14. To reduce electromagnetic emissions and susceptibility, it is imperative that traces from the transceiver to the magnetic sand from the magnetic to the RJ-45 be routed as differential pairs. The objective is to close the loop area formed by the two conductors. The radiated field from the loop or the voltage picked up by the loop by external fields is governed by the field strength and the area formed by the two conductors. Reasonable board design uses 0.005 in.—0.010 in. trace widths separated by 0.010 in. Transmit differential pairs should be routed adjacent to a VDDO power plane.

## Revision history

| Revision | Date | Comment |
|---|---|---|
| V. 1.0 | 5/05/06 | Initial release. |

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