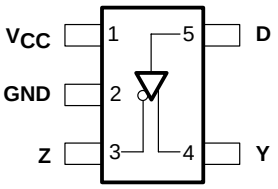
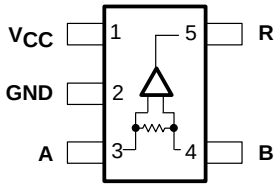
- **Meets or Exceeds the ANSI TIA/EIA-644A Standard**
- **Designed for Signaling Rates† up to:**
  - **630 Mbps Drivers**
  - **400 Mbps Receivers**
- **Operates From a 2.4-V to 3.6-V Supply**
- **Available in SOT–23 and SOIC Packages**
- **Bus-Terminal ESD Exceeds 15 kV**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV Into a 100-Ω Load**
- **Propagation Delay Times**
  - **1.7 ns Typical Driver**
  - **2.5 ns Typical Receiver**
- **Power Dissipation at 200 MHz**
  - **25 mW Typical Driver**
  - **60 mW Typical Receiver**
- **LVDT Receiver Includes Line Termination**
- **Low Voltage TTL (LVTTL) Level Driver Input Is 5-V Tolerant**
- **Driver Is Output High Impedance With V_{CC} < 1.5 V**
- **Receiver Output and Inputs Are High Impedance With V_{CC} < 1.5 V**
- **Receiver Open-Circuit Fail Safe**
- **Differential Input Voltage Threshold Less Than 100 mV**

SN65LVDS1
DBV Package
(TOP VIEW)

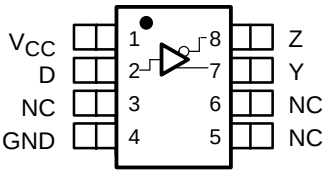


SN65LVDS2 and SN65LVDT2
DBV Package
(TOP VIEW)

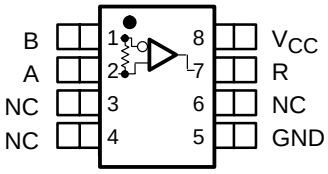


110-Ω Resistor for LVDT Only

SN65LVDS1
D Package
(TOP VIEW)



SN65LVDS2 and SN65LVDT2
D Package
(TOP VIEW)



110-Ω Resistor for LVDT Only

AVAILABLE OPTIONS

PART NUMBER	INTEGRATED TERMINATION	PACKAGE	PACKAGE MARKING
SN65LVDS1DBV		SOT23-5	SAAI
SN65LVDS1D		SOIC-8	LVDS1
SN65LVDS2DBV		SOT23-5	SABI
SN65LVDS2D		SOIC-8	LVDS2
SN65LVDT2DBV	√	SOT23-5	SACI
SN65LVDT2D	√	SOIC-8	LVDT2

description

The SN65LVDS1, SN65LVDS2, and SN65LVDT2 are single, low-voltage, differential line drivers and receivers in the small-outline transistor package. The outputs comply with the TIA/EIA-644A standard and provide a minimum differential output voltage magnitude of 247 mV into a 100-Ω load at signaling rates up to 630 Mbps for drivers and 400 Mbps for receivers.

When the SN65LVDS1 is used with an LVDS receiver (such as the SN65LVDT2) in a point-to-point connection, data or clocking signals can be transmitted over printed-circuit-board traces or cables at very high rates with very low electromagnetic emissions and power consumption. The packaging, low power, low EMI, high ESD tolerance, and wide supply voltage range make the device ideal for battery-powered applications.

The SN65LVDS1, SN65LVDS2, and SN65LVDT2 are characterized for operation from –40°C to 85°C.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second)

Function Tables

DRIVER

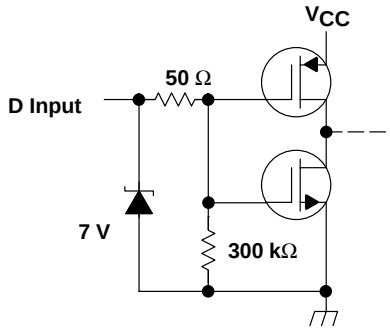
INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

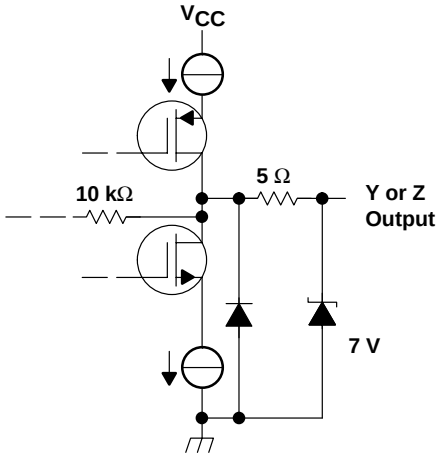
RECEIVER

INPUTS	OUTPUT
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

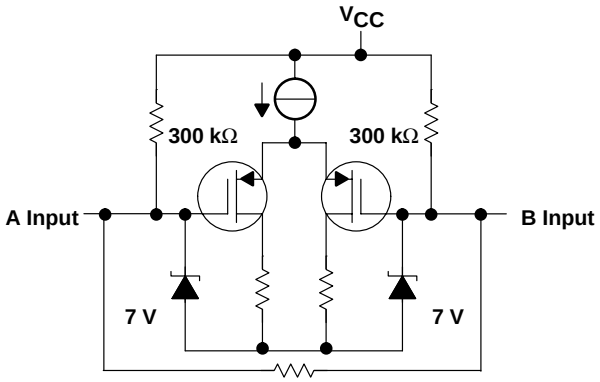
H = high level, L = low level , ? = indeterminate

driver equivalent input and output schematic diagrams

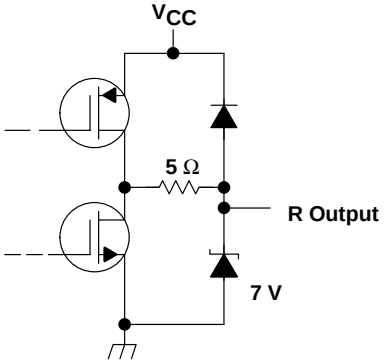




receiver equivalent input and output schematic diagrams



110-Ω LVDT Only



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Input voltage range: (D) . . . . . –0.5 V to V_{CC} + 2 V
(A, B, Y, or Z) . . . . . –0.5 V to V_{CC} + 0.5 V
$|V_{ID}|$ (LVDT2) . . . . . 1 V
Electrostatic discharge: A, B, Y, Z, and GND (see Note 2) . . . . . CLass 3, A:15 kV, B:600 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 250°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114–A.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	402 mW
DBV	385 mW	3.1 mW/°C	200 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-K) and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.4	3.3	3.6	V
High-level input voltage, V_{IH}	2		5	V
Low-level input voltage, V_{IL}	0		0.8	V
Operating free-air temperature, T_A	–40		85	°C
Magnitude of differential input voltage, $\|V_{ID}\|$	0.1		0.6	V
Input voltage (any combination of input or common-mode voltage)	0		V_{CC}– 0.8	V

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN‡	TYP†	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, 2.4 ≤ V_{CC} <3 V	200	350	454	mV
		R_L = 100 Ω, 3 ≤ V_{CC} <3.6 V	247	350	454	
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	See Figure 2	–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 2	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			25	100	mV
I_{CC}	Supply current	V_I = 0 V or V_{CC}, No load		2	4	mA
		V_I = 0 V or V_{CC}, R_L = 100 Ω		5.5	8	
I_{IH}	High-level input current	V_{IH} = 5 V		2	20	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V		2	10	μA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V		3	10	mA
		V_{OD} = 0 V			10	
$I_{O(OFF)}$	Power-off output current	V_{CC} = 0 V, V_O = 3.6 V	–1		1	μA
C_i	Input capacitance	V_I = 0.4 Sin (4E6πt)+0.5 V		3		pF

† All typical values are at 25°C and with a 3.3-V supply.
‡ The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 5		1.5	3.1	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.8	3.1	ns
t_r	Differential output signal rise time			0.6	1	ns
t_f	Differential output signal fall time			0.7	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)‡			0.3		ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN‡	TYP†	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold		See Figure 3			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold			–100			
V_{OH}	High-level output voltage		I_{OH} = –8 mA, V_{CC} = 2.4 V	1.9			V
			I_{OH} = –8 mA, V_{CC} = 3 V	2.4			
V_{OL}	Low-level output voltage		I_{OL} = 8 mA		0.25	0.4	V
I_{CC}	Supply current		No load, Steady state		4	7	mA
I_I	Input current (A or B inputs)	LVDS2	V_I = 0 V, other input = 1.2 V	–20		–2	µA
			V_I = 2.2 V, other input = 1.2 V, V_{CC} = 3.0 V		–3	–1.2	
		LVDT2	V_I = 0 V, other input open	–40		–4	
			V_I = 2.2 V, other input open, V_{CC} = 3.0 V		–6	–2.4	
I_{ID}	Differential input current ($I_{IA} – I_{IB}$)	LVDS2	V_{IA} = 2.4 V V_{IB} = 2.3 V	–2		2	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	LVDS2	V_{CC} = 0 V, $V_{IA} = V_{IB}$ = 2.4 V			20	µA
		LVDT2	V_{CC} = 0 V, $V_{IA} = V_{IB}$ = 2.4 V			40	
R_T	Differential input resistance	LVDT2	V_{IA} = 2.4 V V_{IB} = 2.2 V	90	111	132	Ω

† All typical values are at 25°C and with a 2.7-V supply.
‡ The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 6	1.4	2.6	3.6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.4	2.5	3.6	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} – t_{pLH} \rvert$)‡			0.1	0.6	ns
t_r	Output signal rise time			0.8	1.4	ns
t_f	Output signal fall time			0.8	1.4	ns

† All typical values are at 25°C and with a 2.7-V supply.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

PARAMETER MEASUREMENT INFORMATION

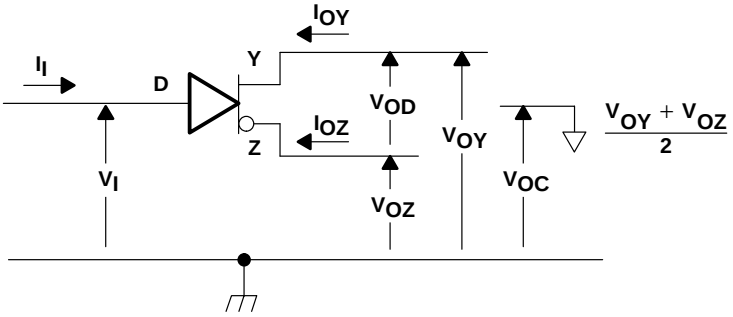
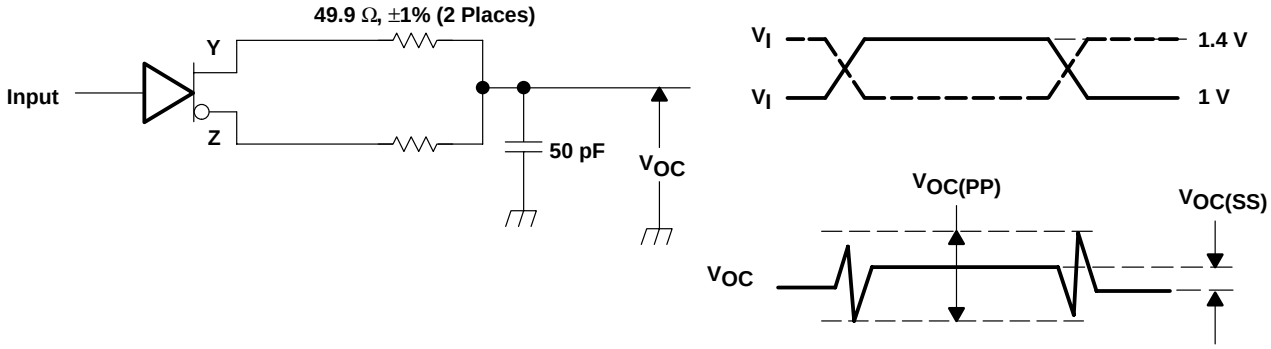


Figure 1. Driver Voltage and Current Definitions



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 2. Driver Test Circuit and Definitions for the Driver Common-Mode Output Voltage

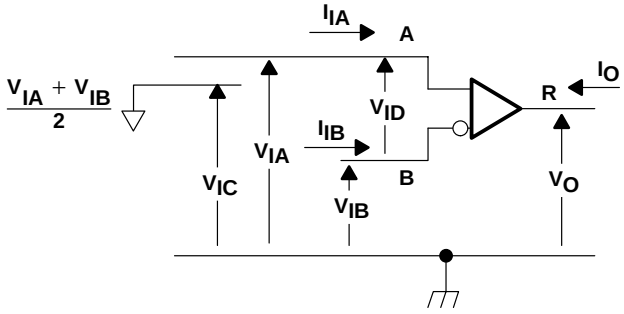
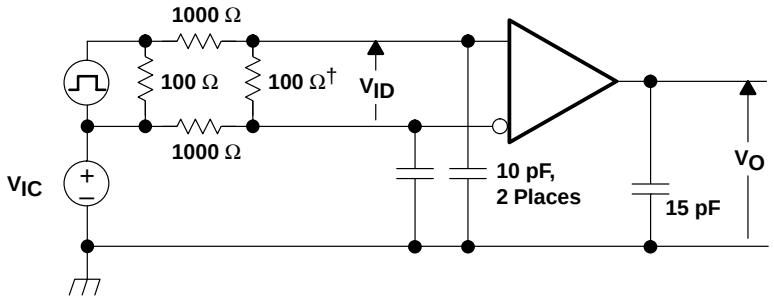


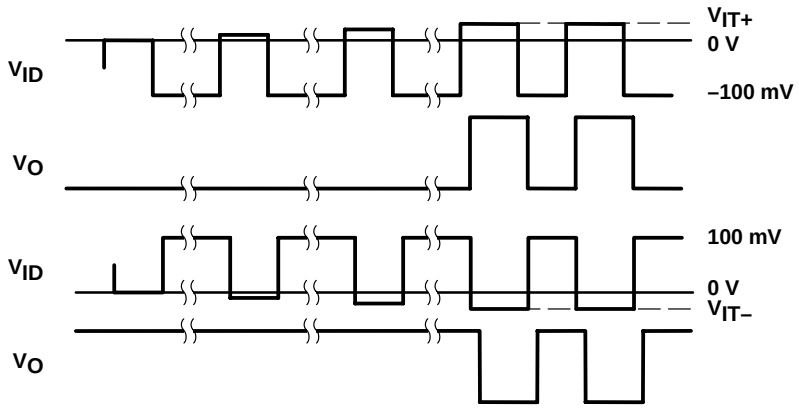
Figure 3. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION



† Remove for testing LVDT device.

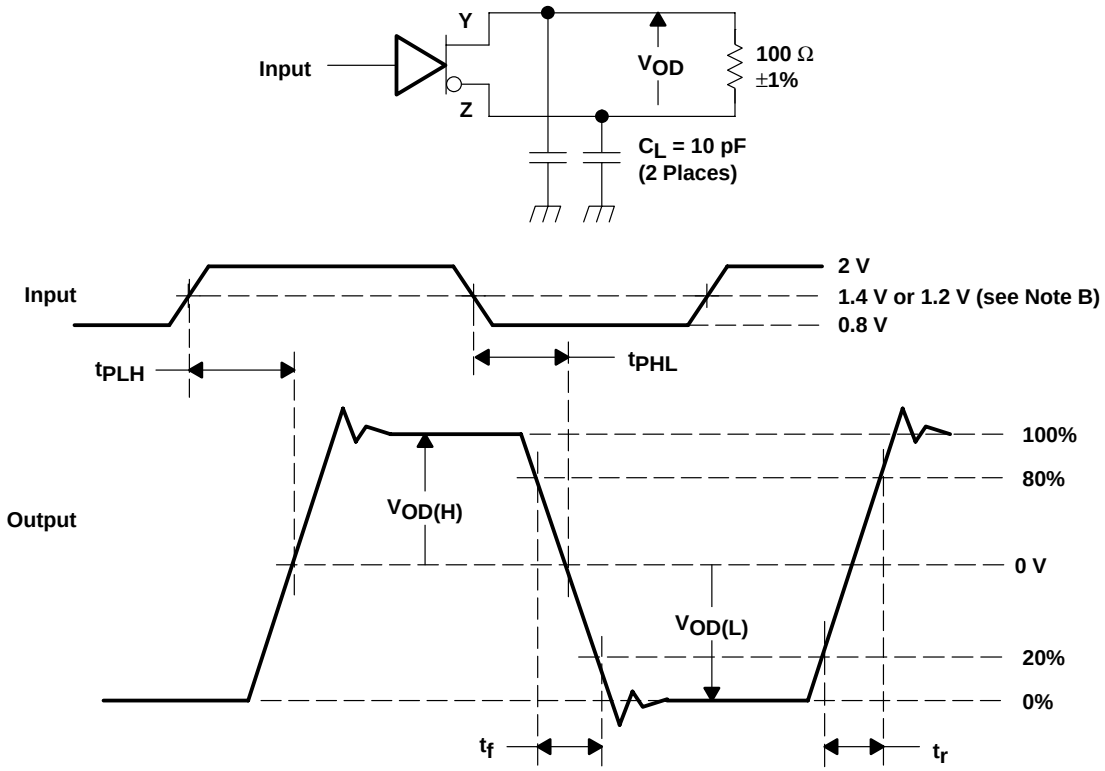
NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of < 1 ns.



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

Figure 4. V_{IT+} and V_{IT-} Input Voltage Threshold Test Circuit and Definitions

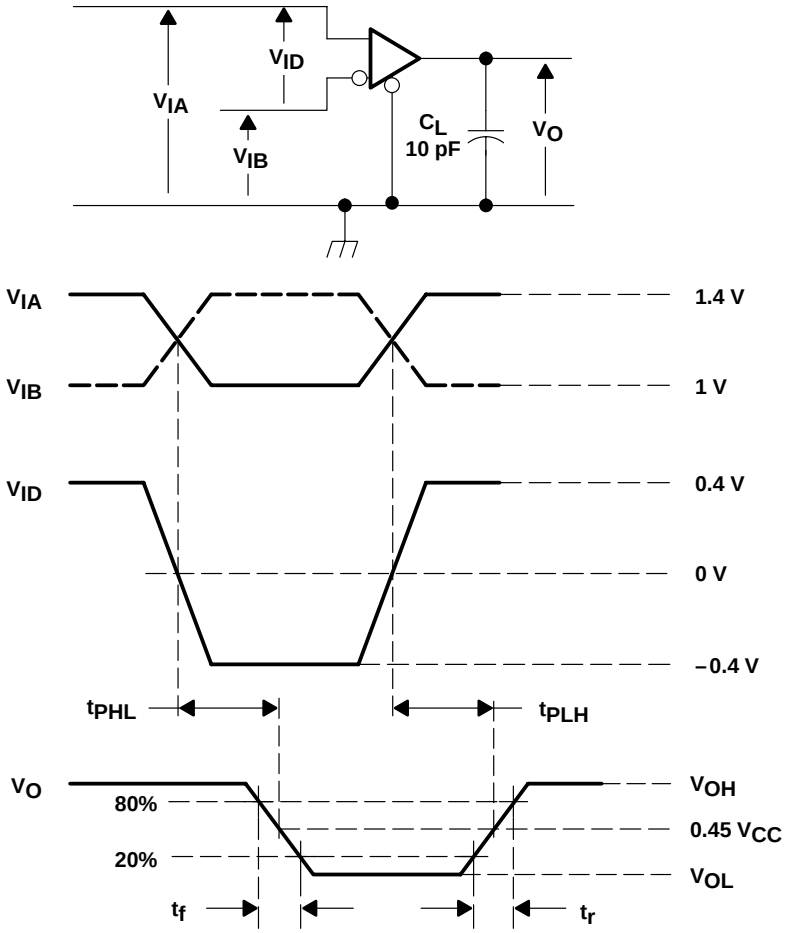
PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.
B. This point is 1.4 V with V_{CC} = 3.3 V or 1.2 V with V_{CC} = 2.7 V

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 6. Receiver Timing Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

DRIVER HIGH-TO-LOW LEVEL PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

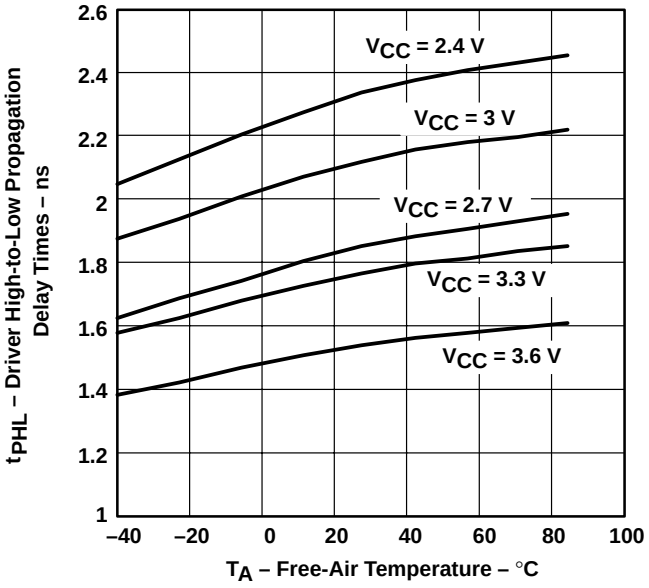


Figure 7

DRIVER LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

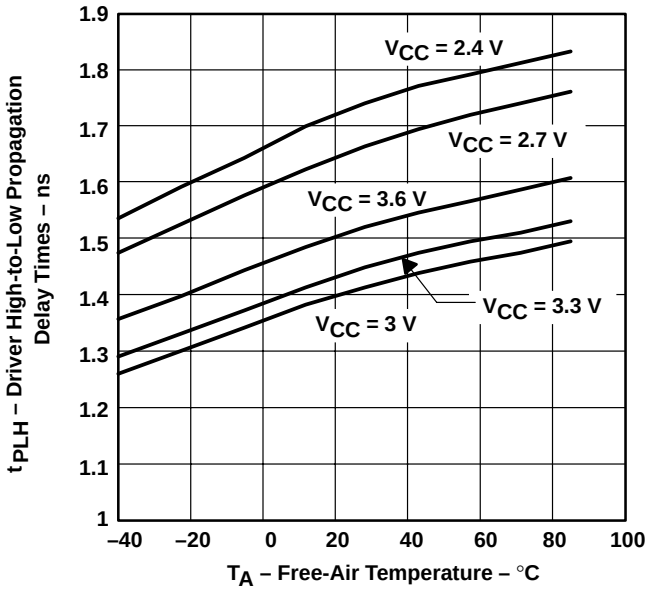


Figure 8

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

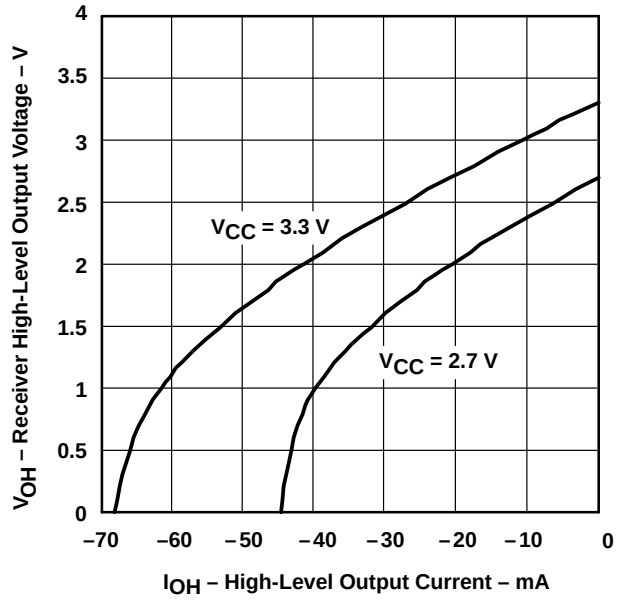


Figure 9

RECEIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

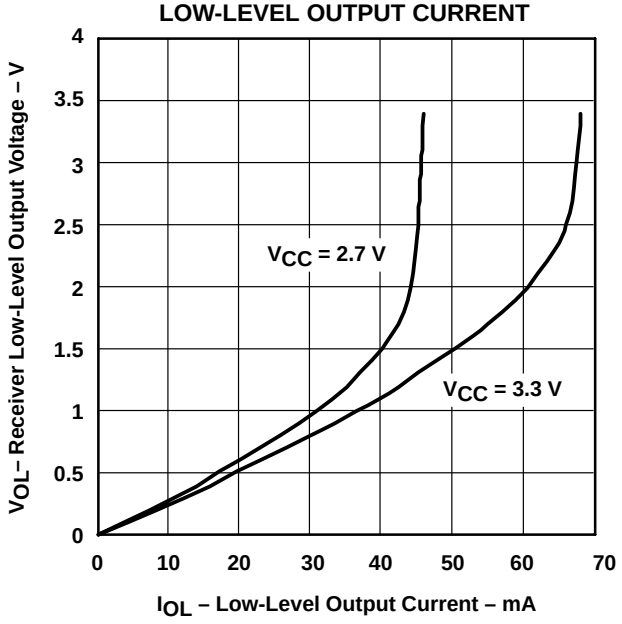


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER HIGH-TO-LOW LEVEL PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

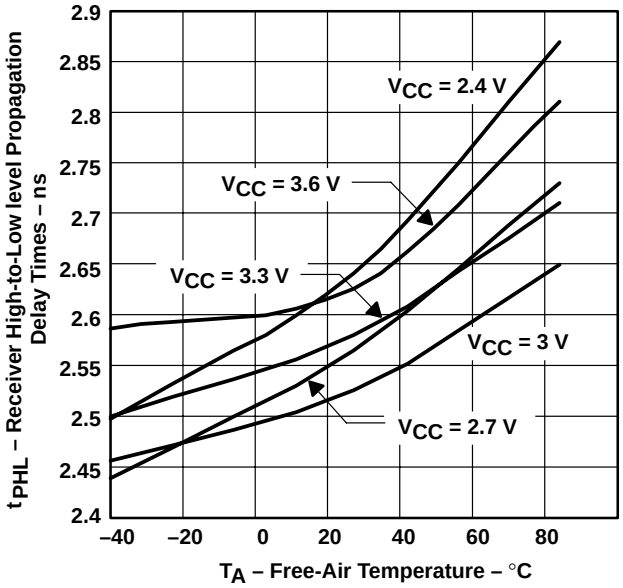


Figure 11

RECEIVER LOW-TO-HIGH LEVEL PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

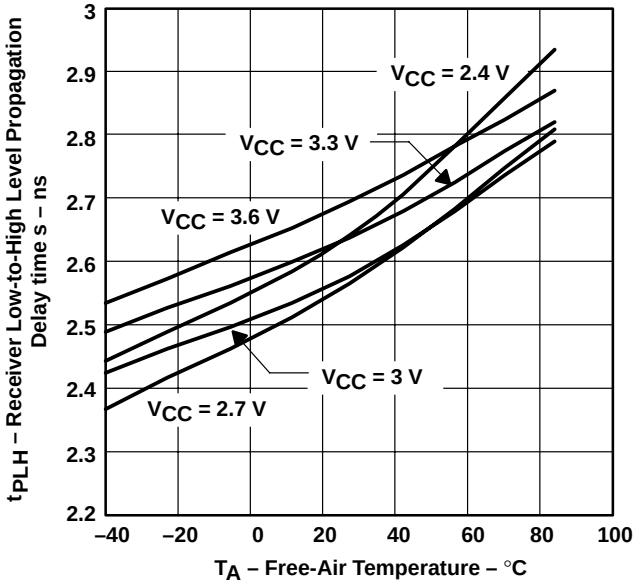


Figure 12

APPLICATION INFORMATION

fail-safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. However, TI's LVDS receiver is different in how it handles the open-input circuit situation.

Open circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 13. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level regardless of the differential input voltage.

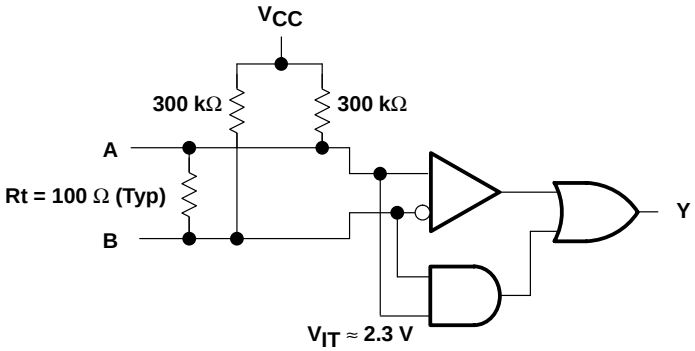
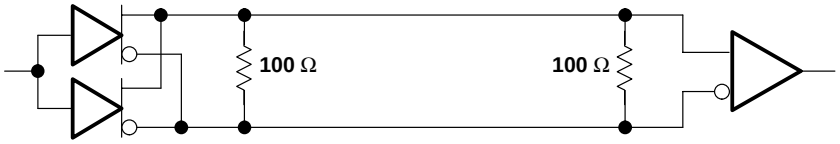


Figure 13. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

APPLICATION INFORMATION

Parallel Terminated



Point to Point

Multidrop

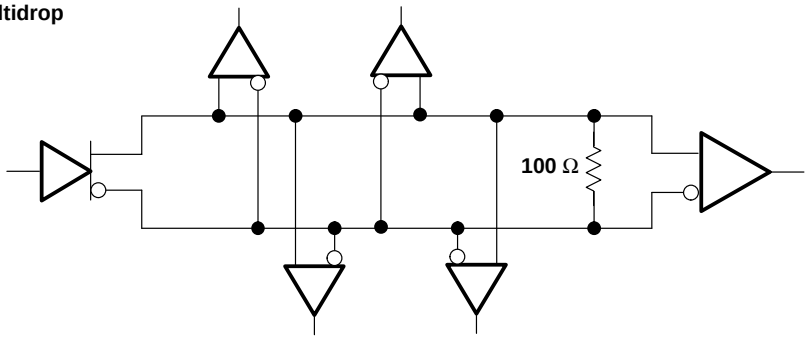
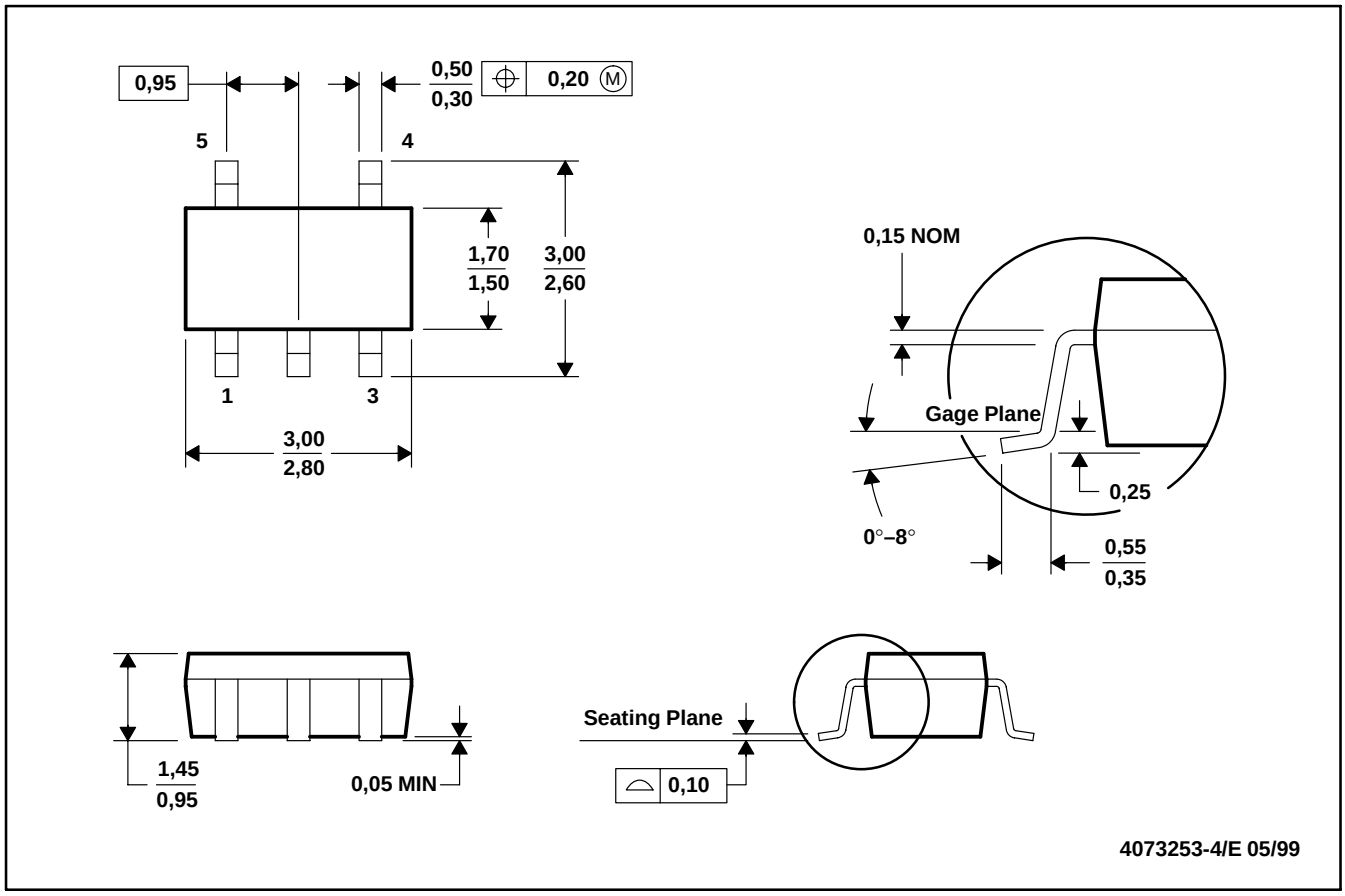


Figure 14. Typical Application Circuits

MECHANICAL INFORMATION

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**

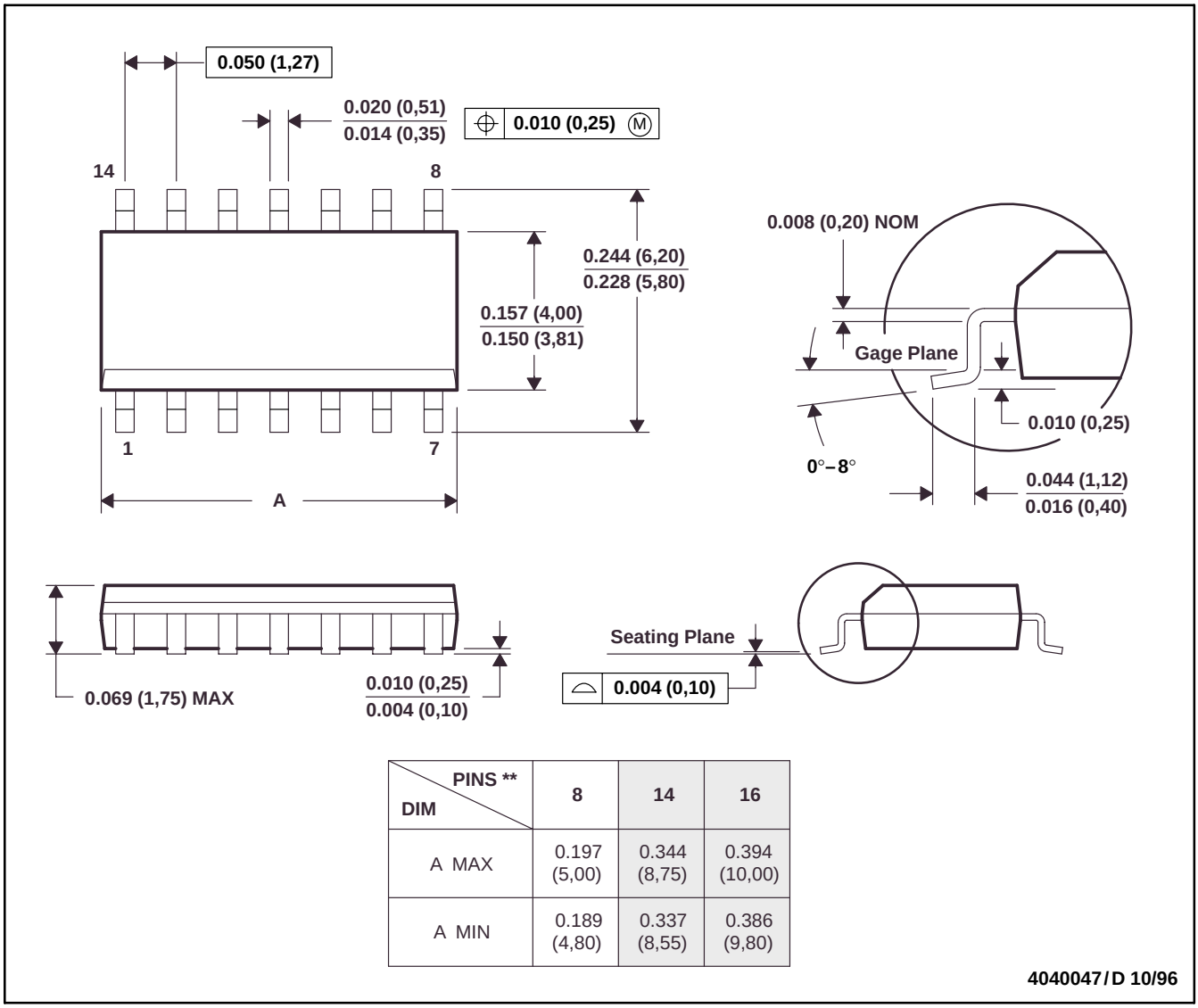


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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