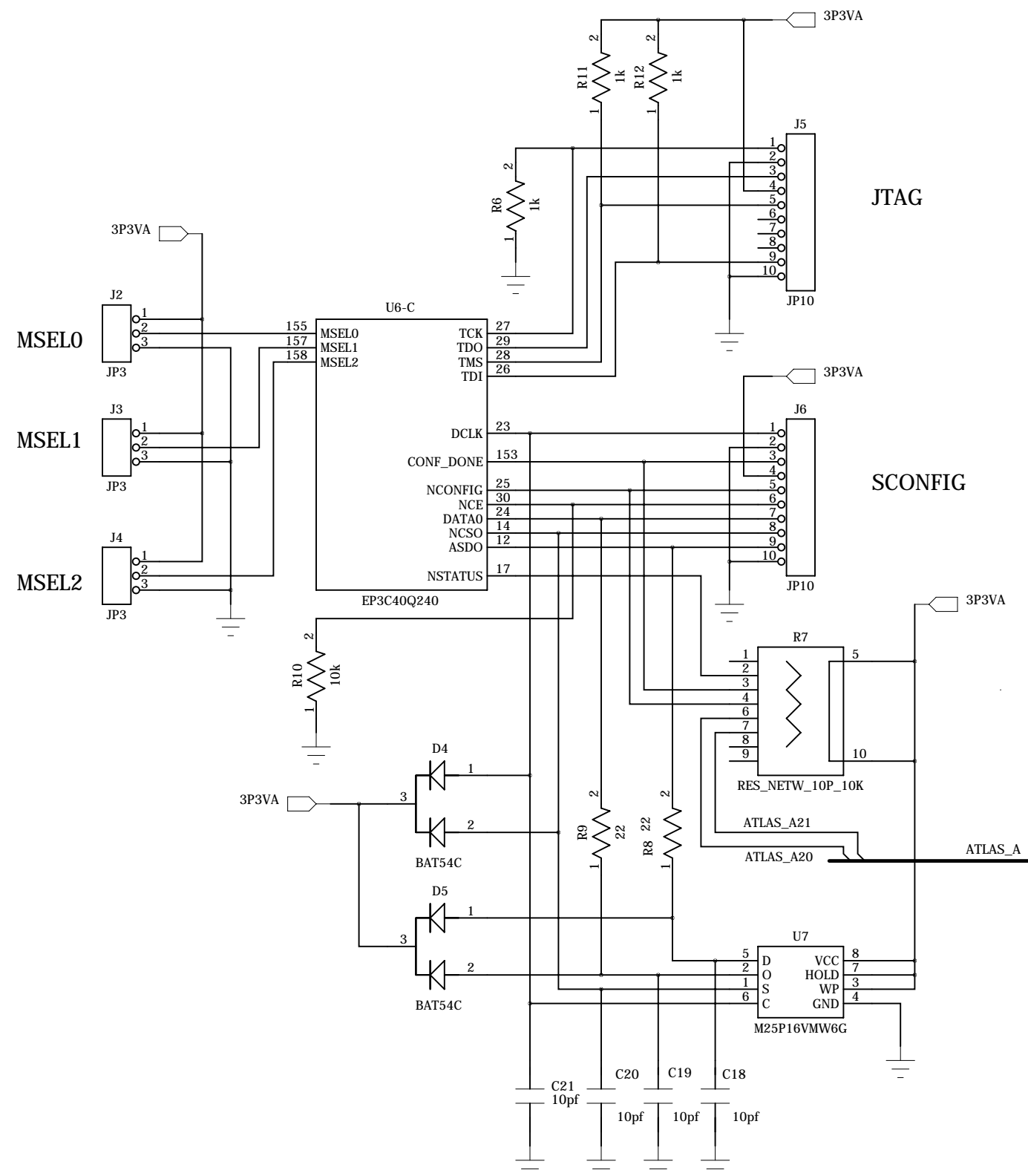


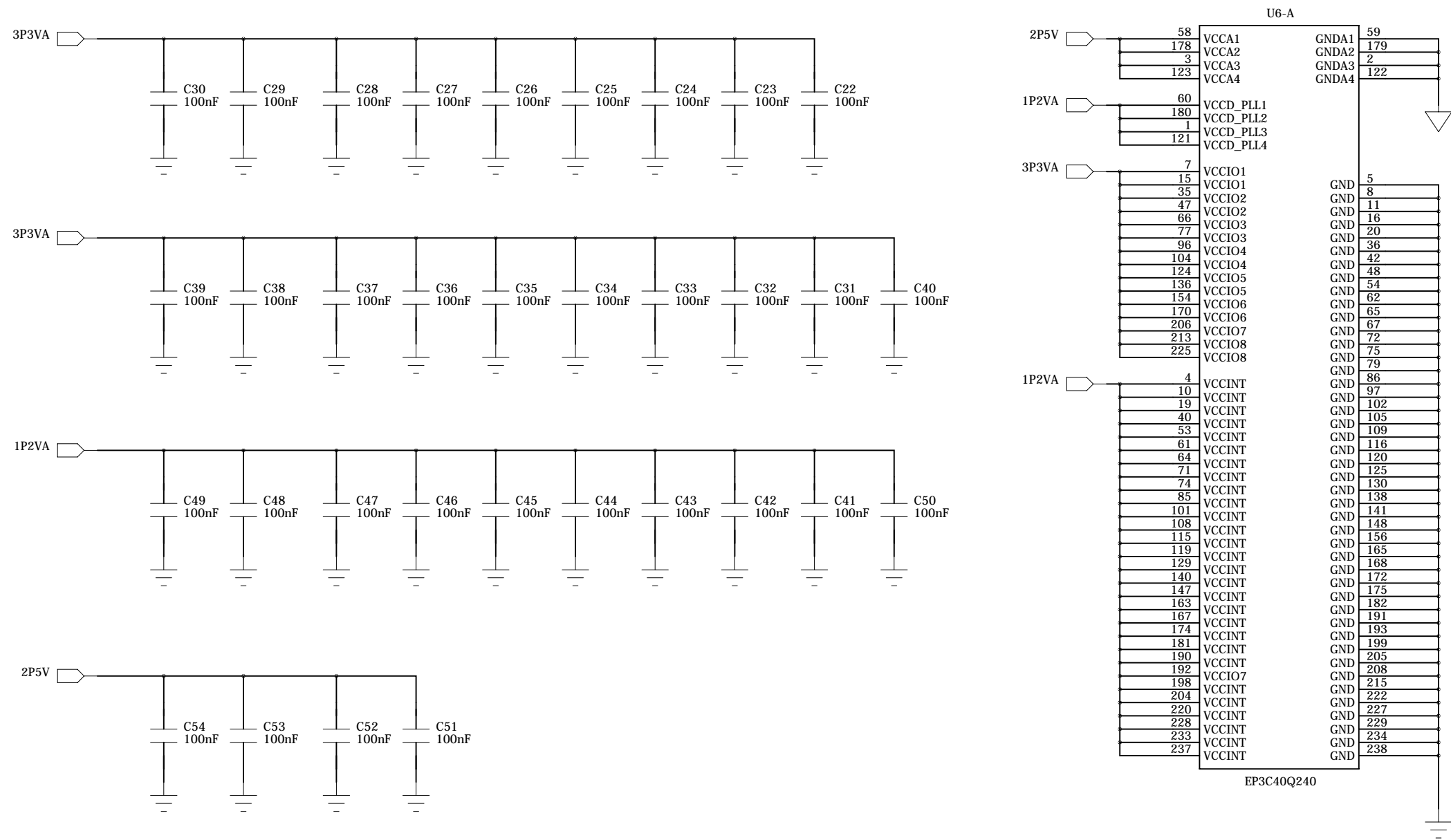
OpenHPSDR

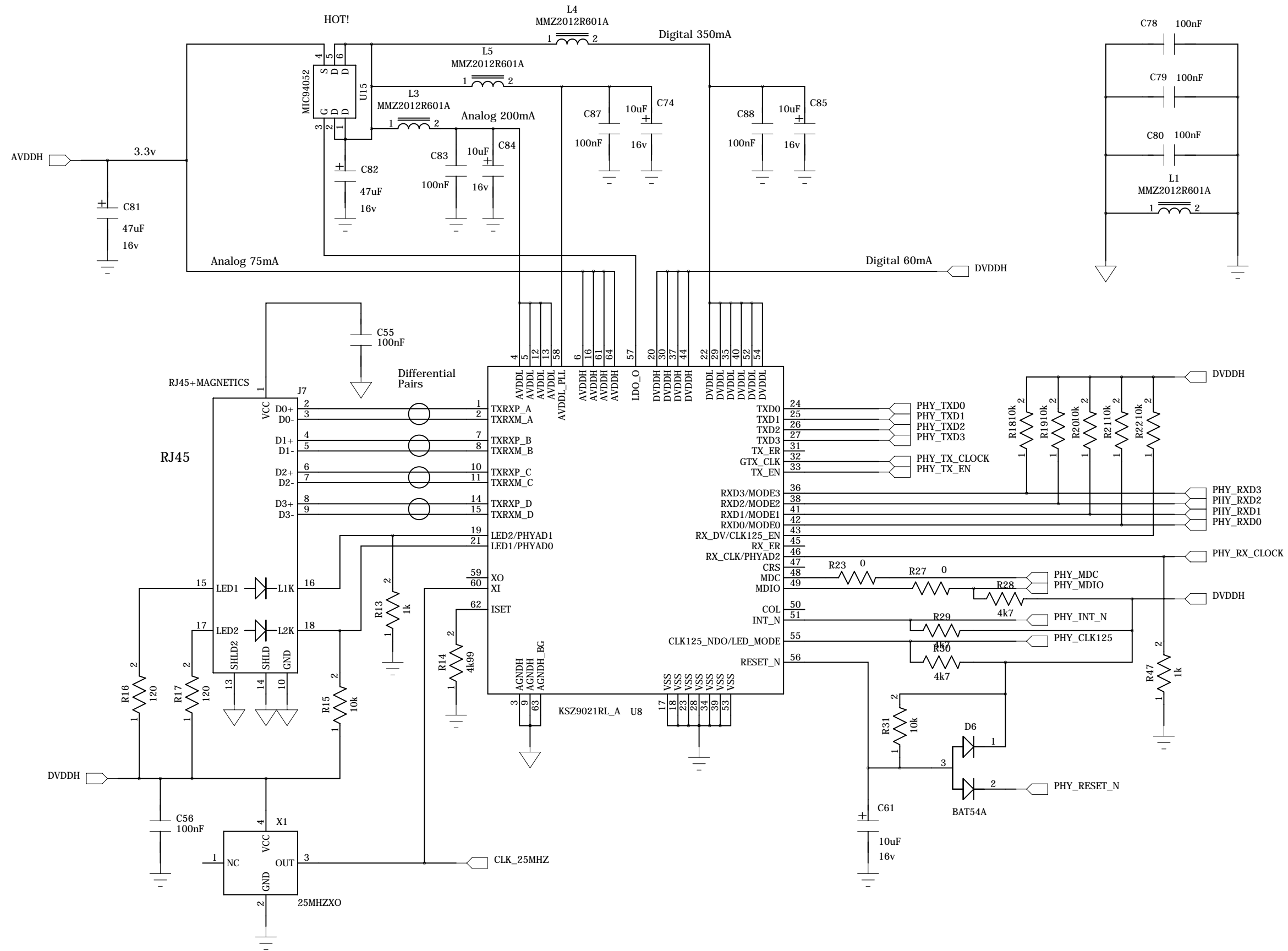
<Power Supplies>

<OzyII>

	MSEL2	MSEL1	MSEL0
AS	0	1	0
PS	1	0	0
FPP	1	1	0
JTAG	X	X	X







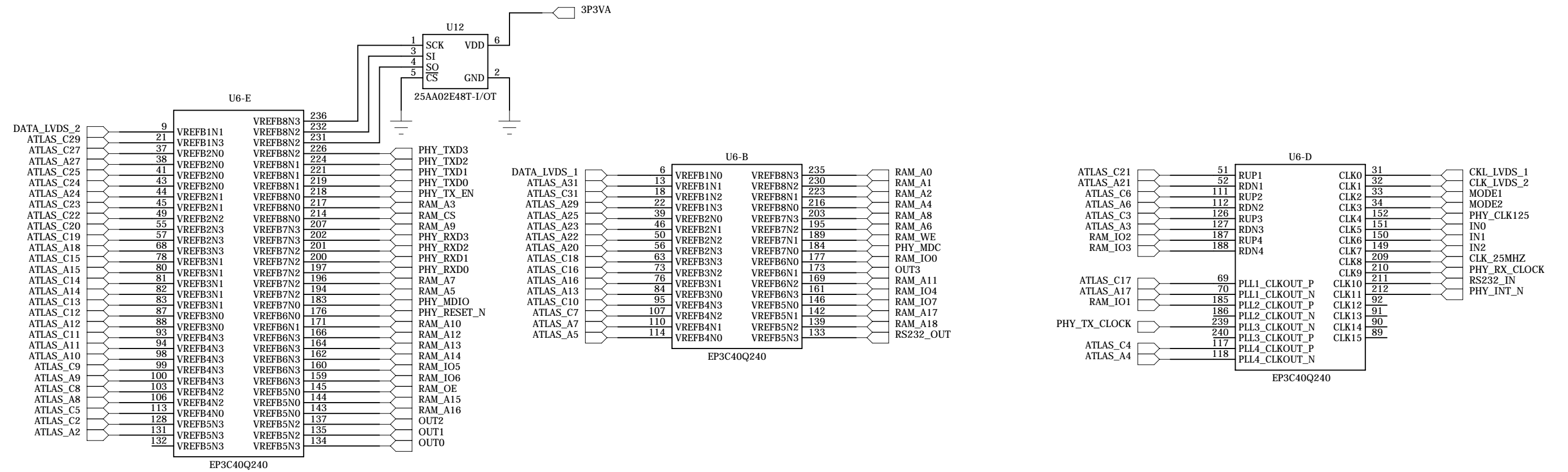
OpenHPSDR

<PHY Interface>

<OzyII>

FPGA pin 1 top left

PHY pin 1 bottom right



OpenHPSDR

<FPGA IO>

<OzyII>

